

FIG. 1A

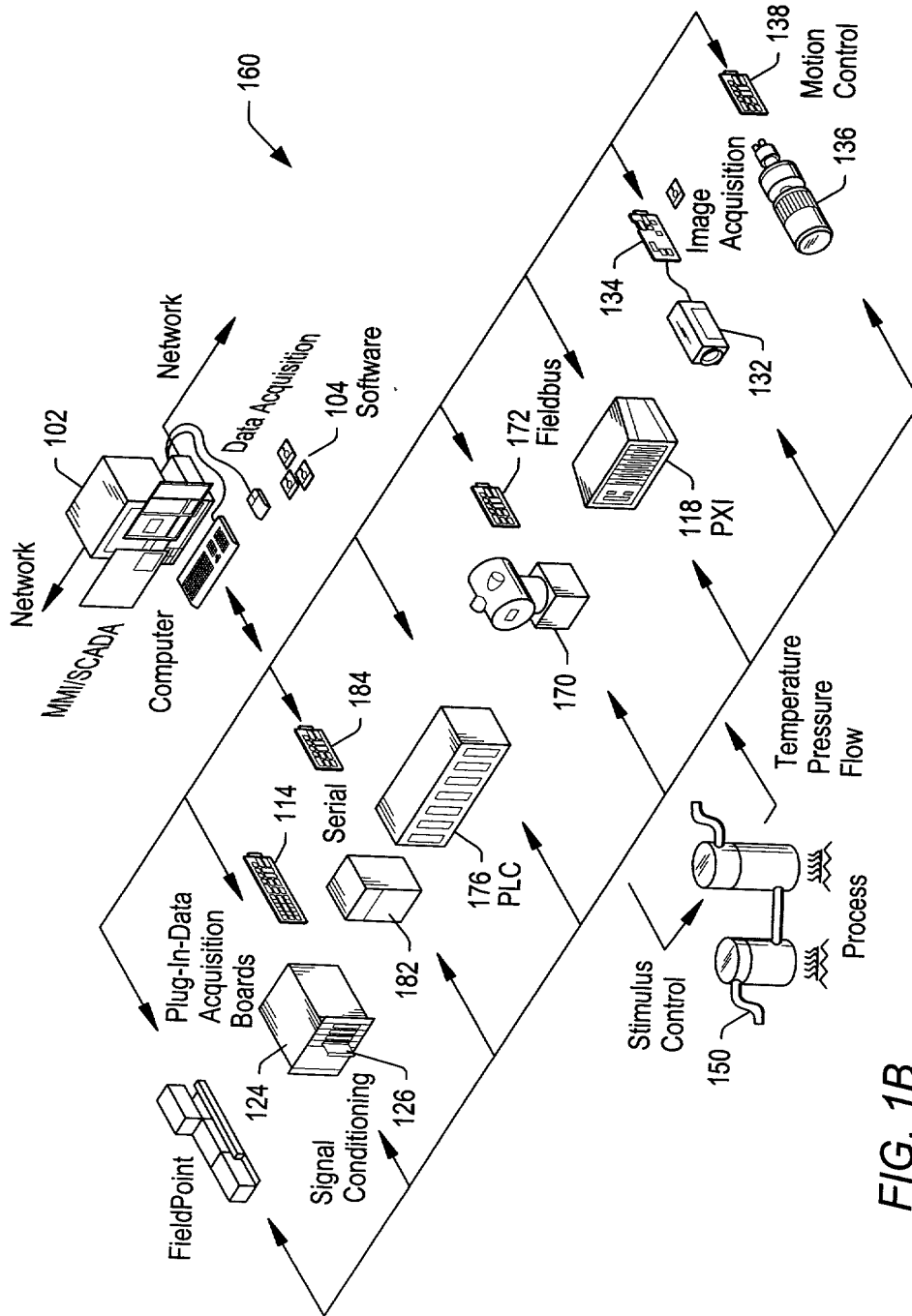


FIG. 1B

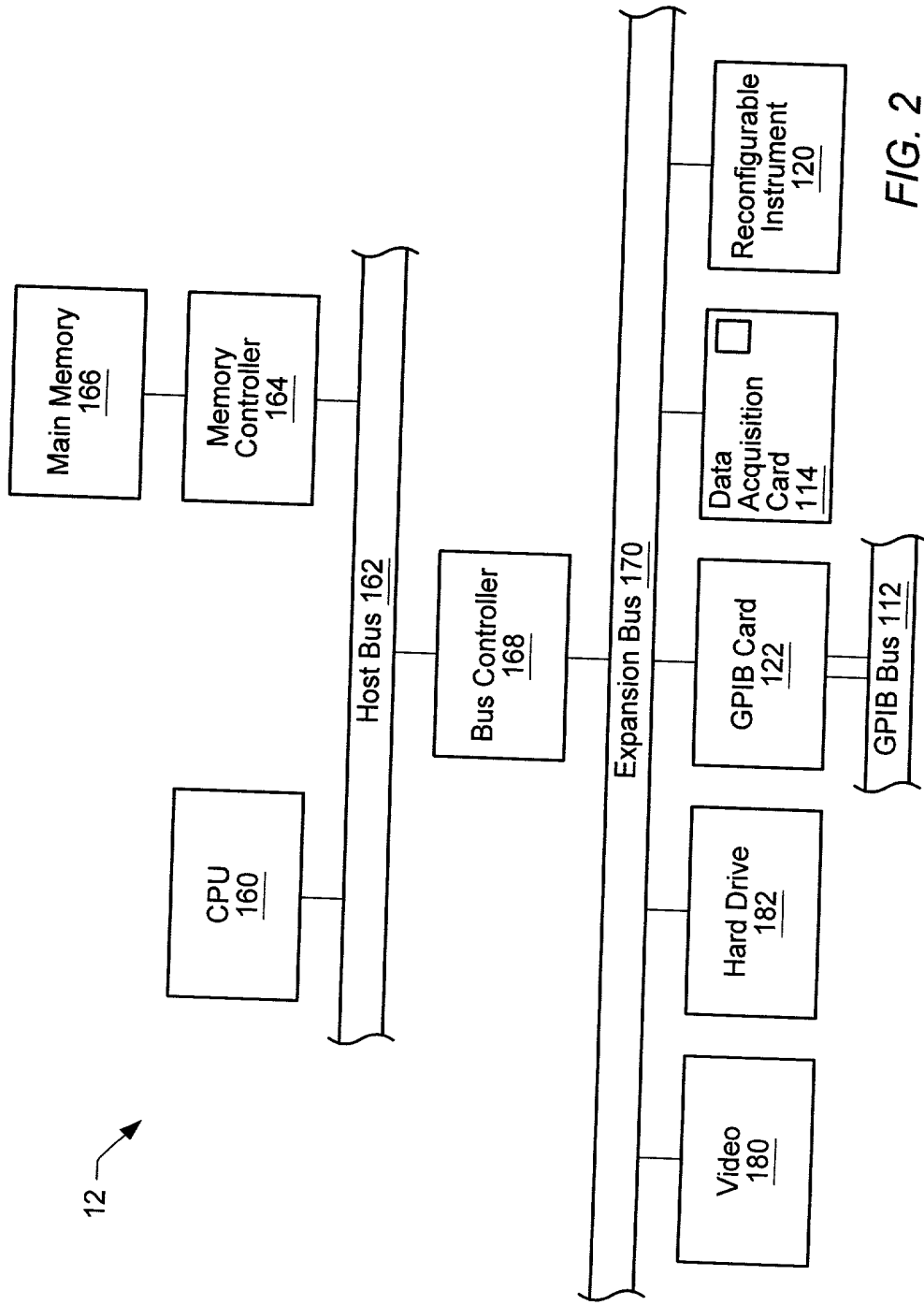


FIG. 2

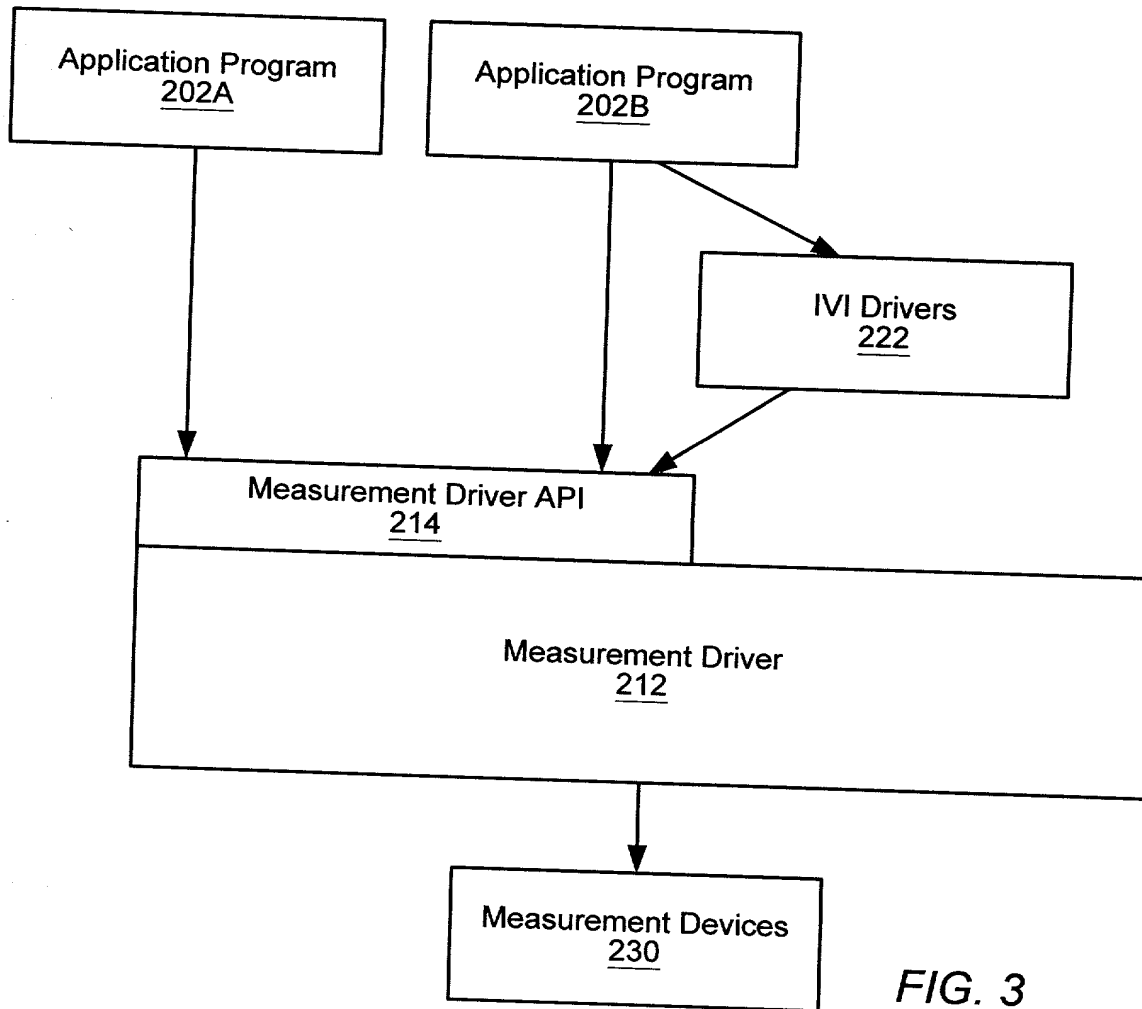


FIG. 3

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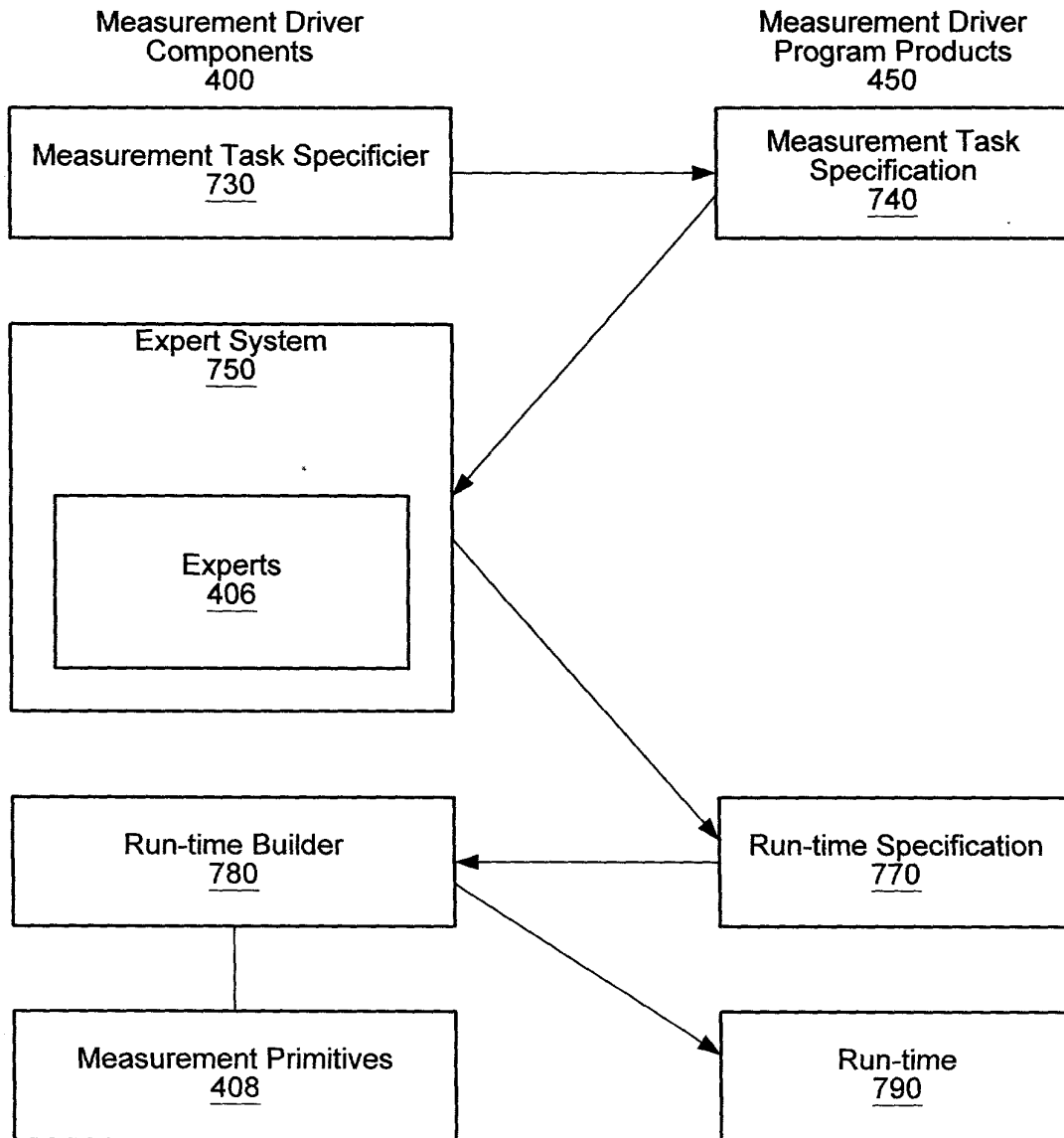


FIG. 4

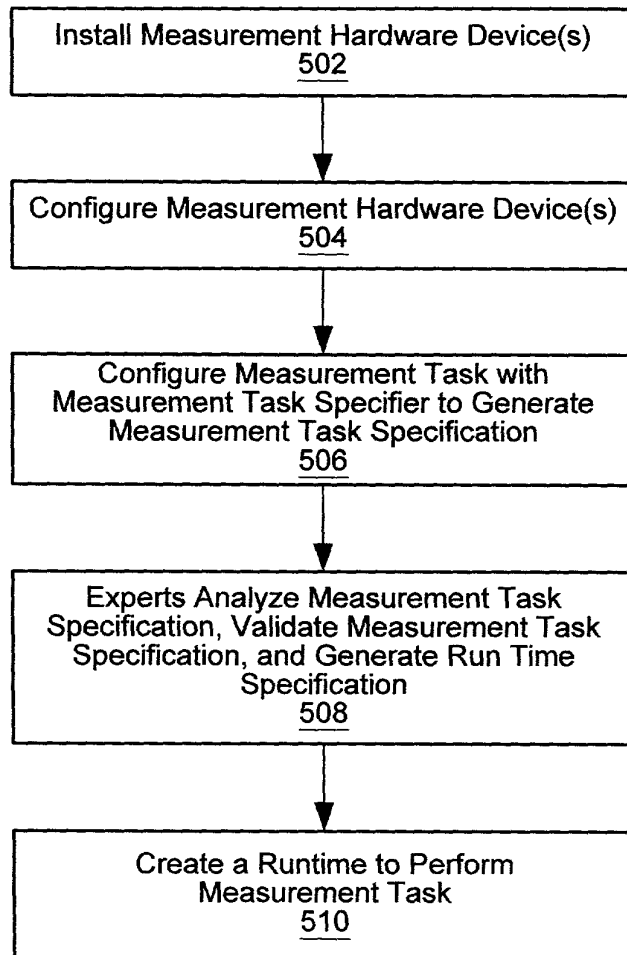


FIG. 5

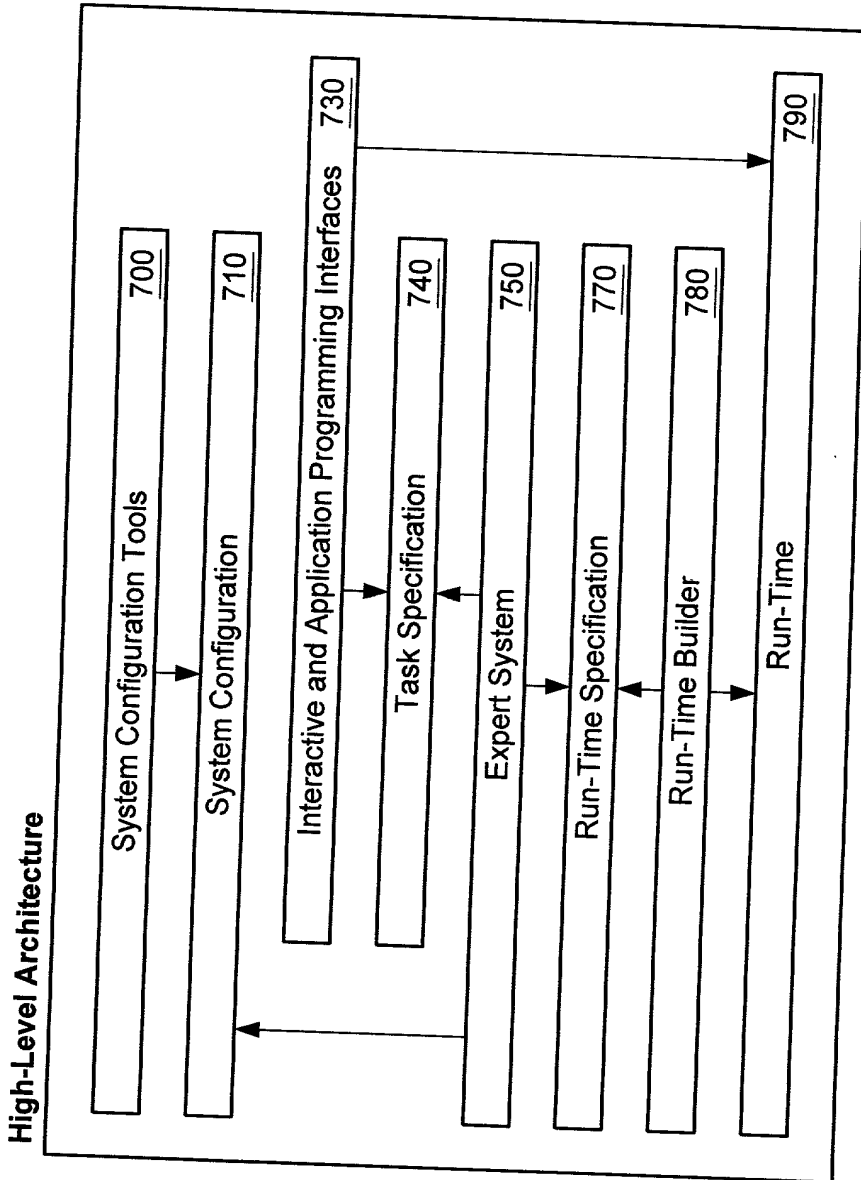


FIG. 6

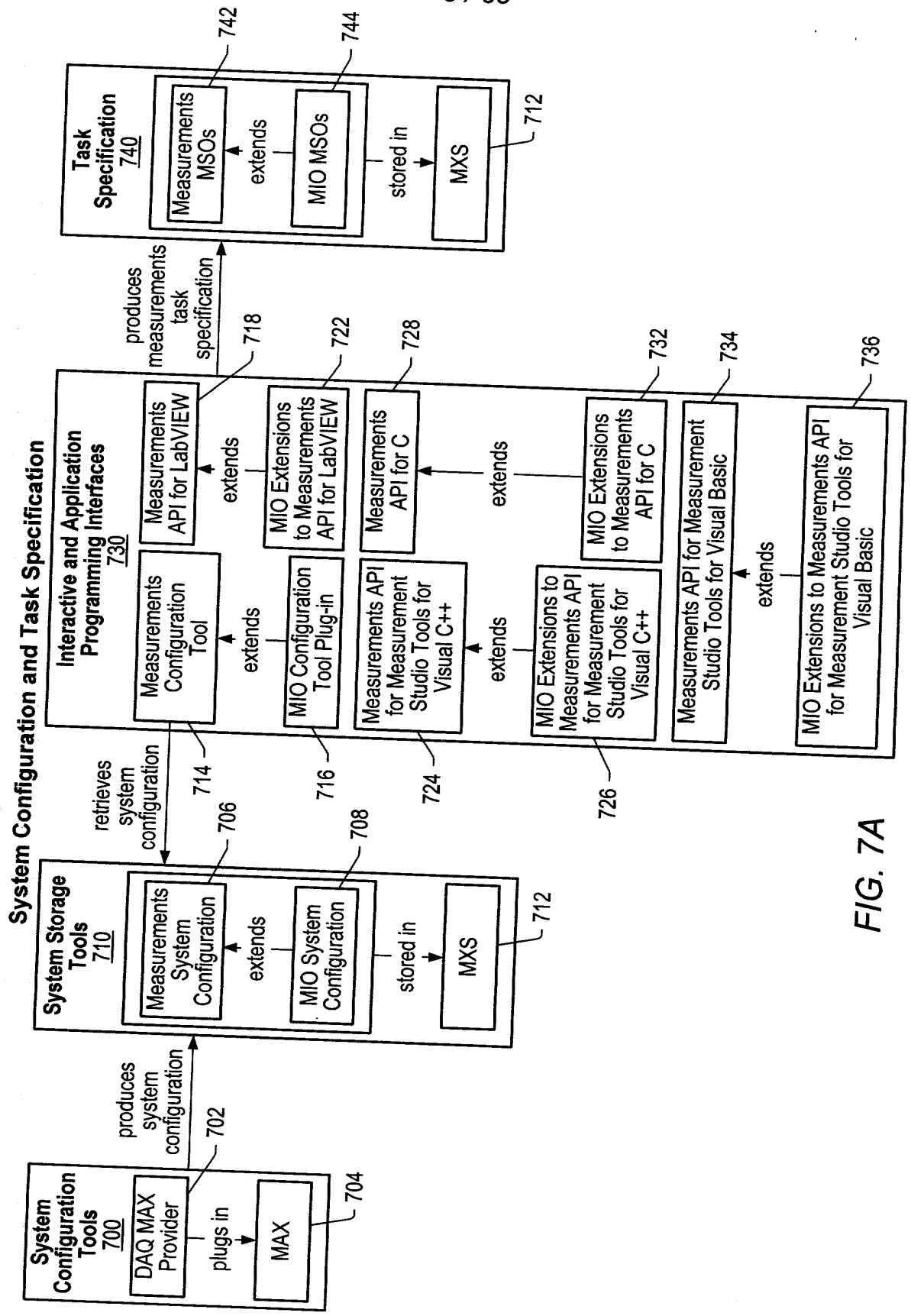


FIG. 7A

20250001 20250001 20250001

Compiling Task Specification to Task Run-time Specification

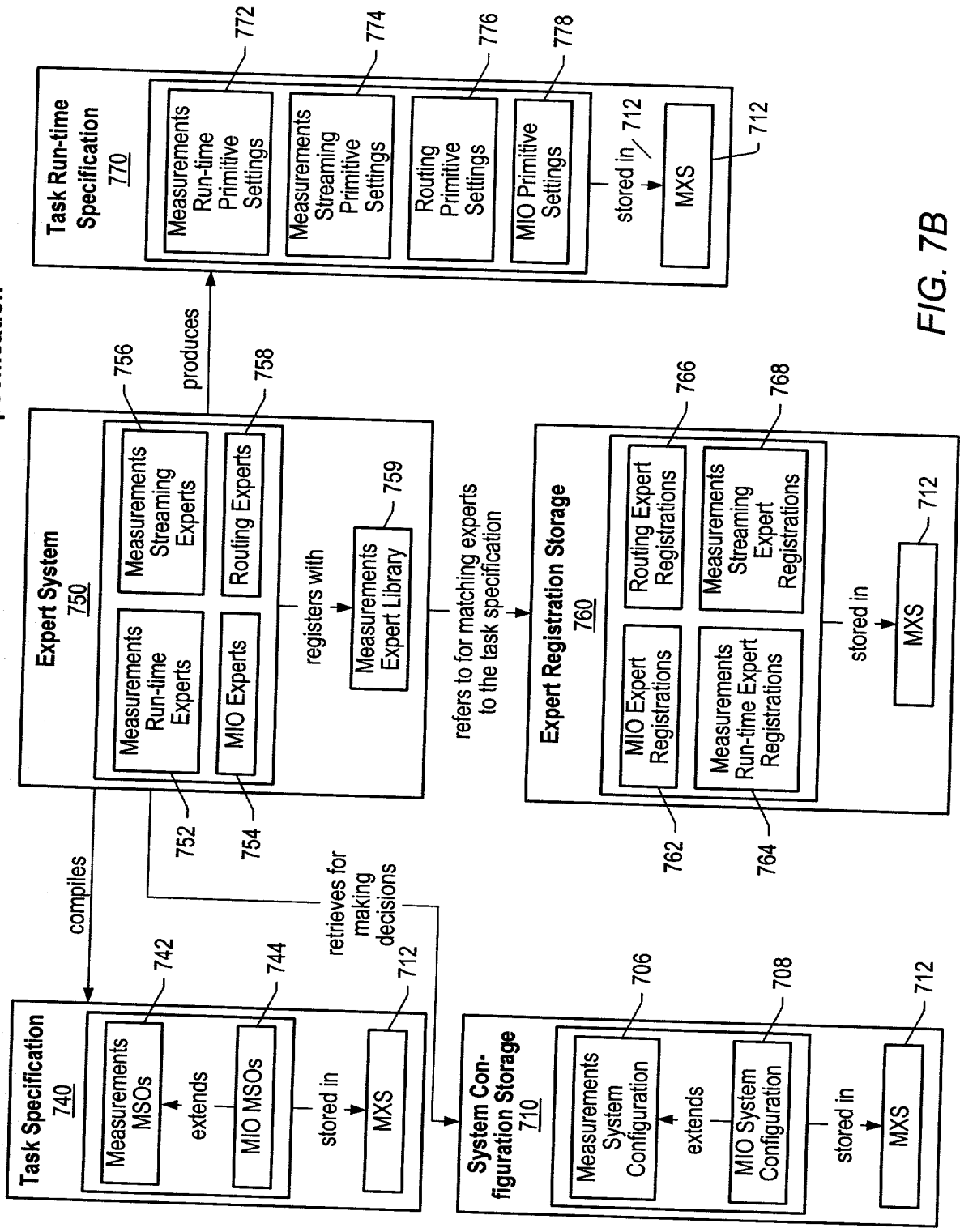


FIG. 7B

Building Task Run-time from Task Run-time Specification

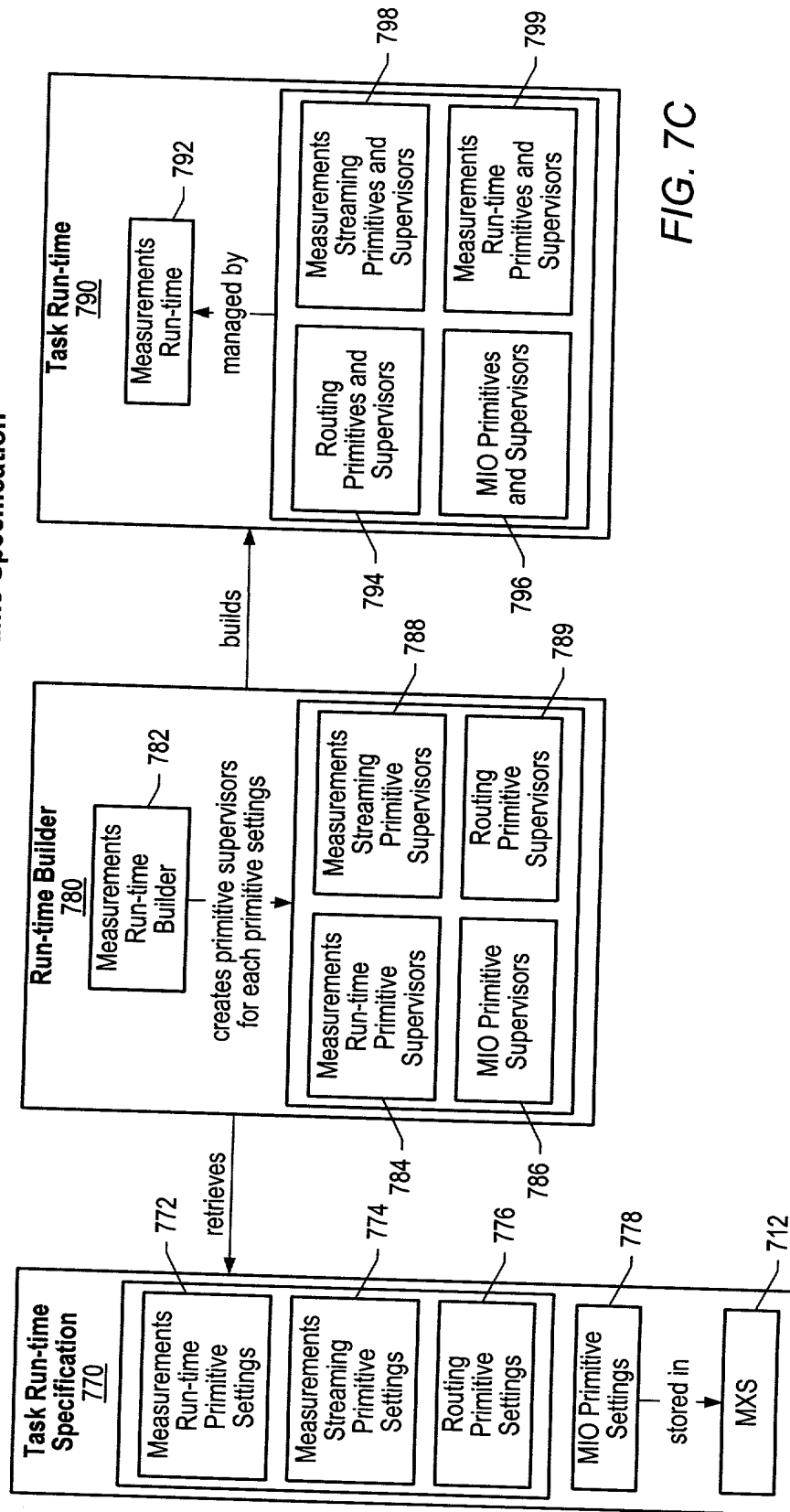


FIG. 7C

Executing Tasks

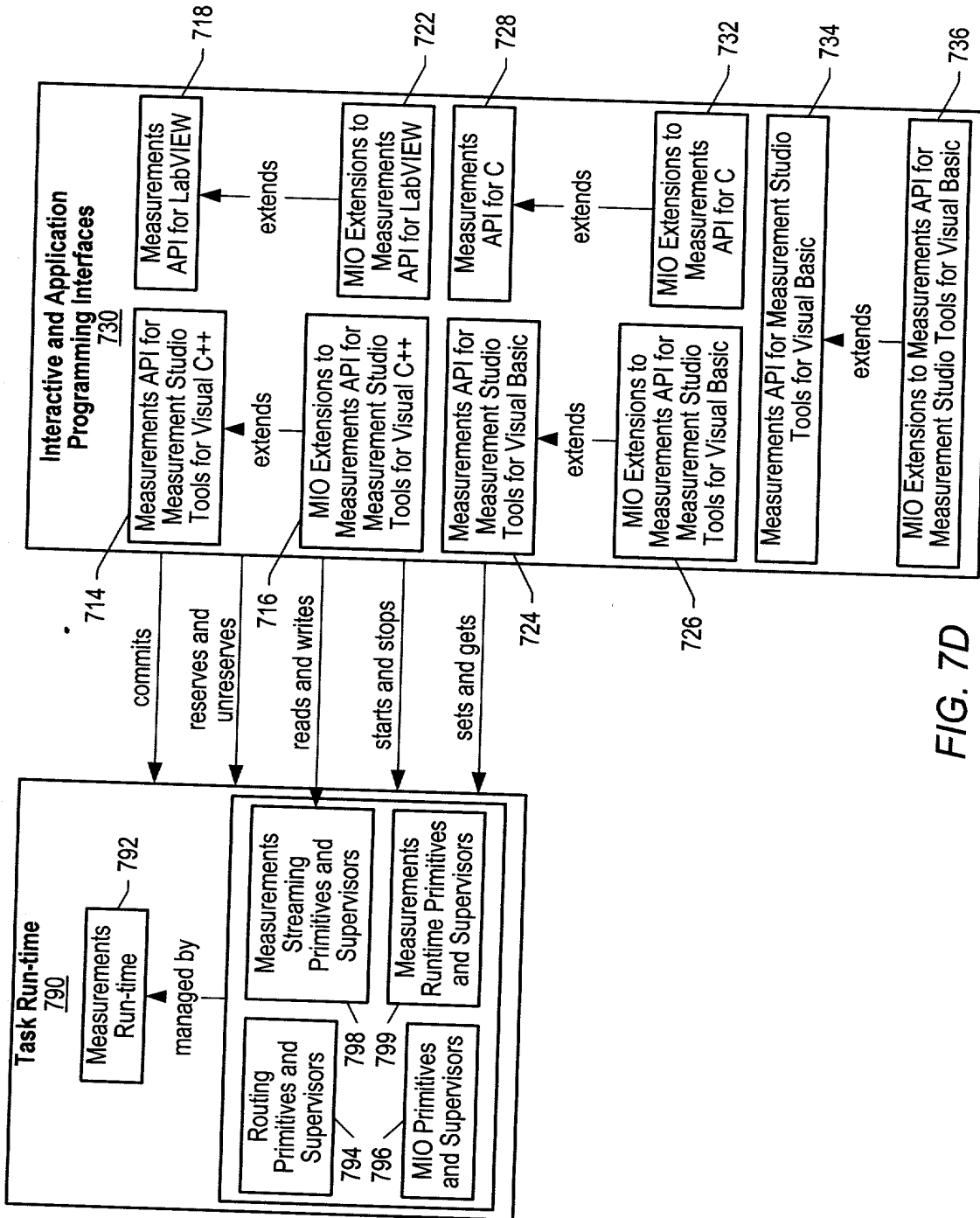


FIG. 7D

Packages for System Configuration and Task Specification

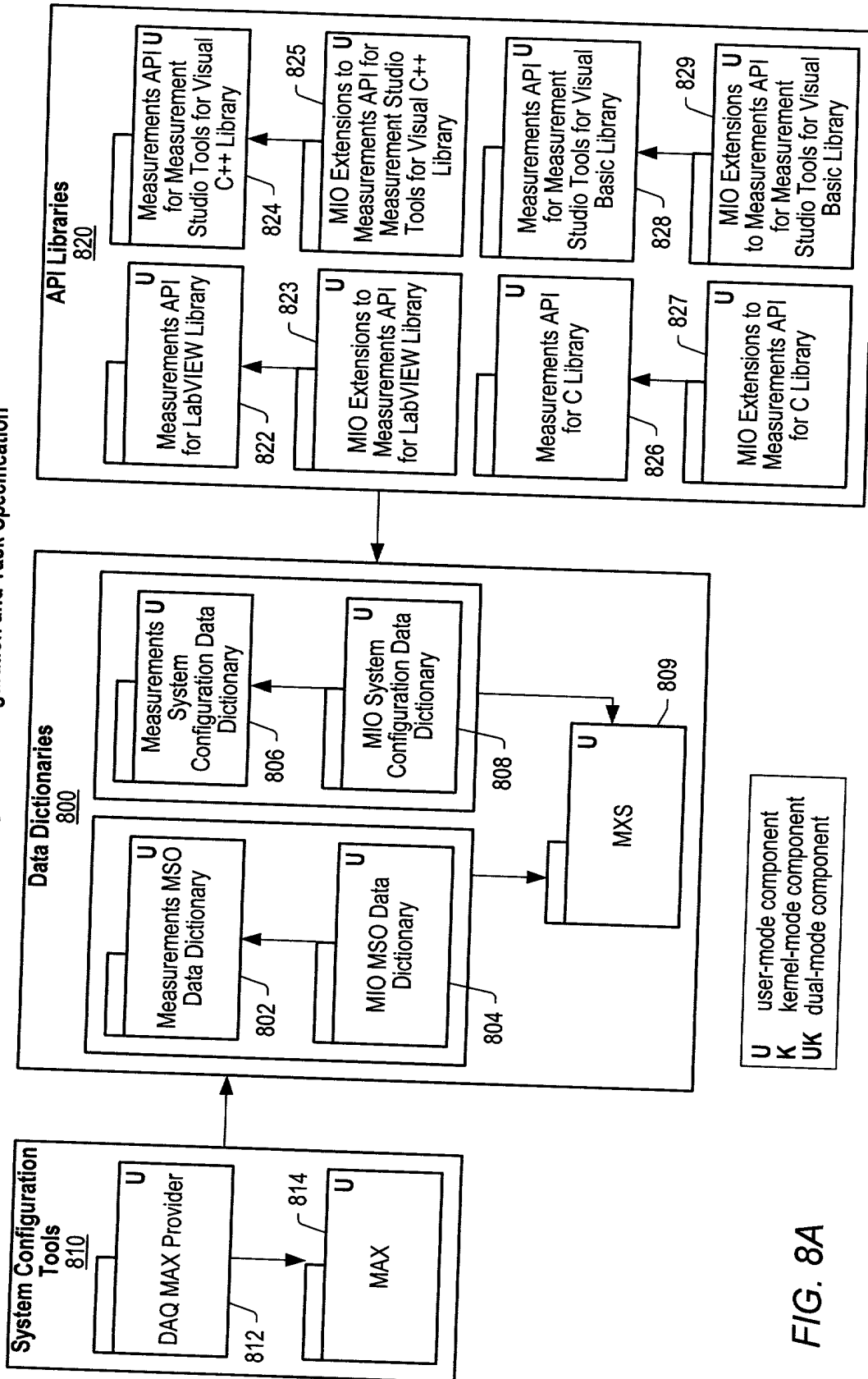


FIG. 8A

Packages for Compiling Task Specification to Run-time Specification

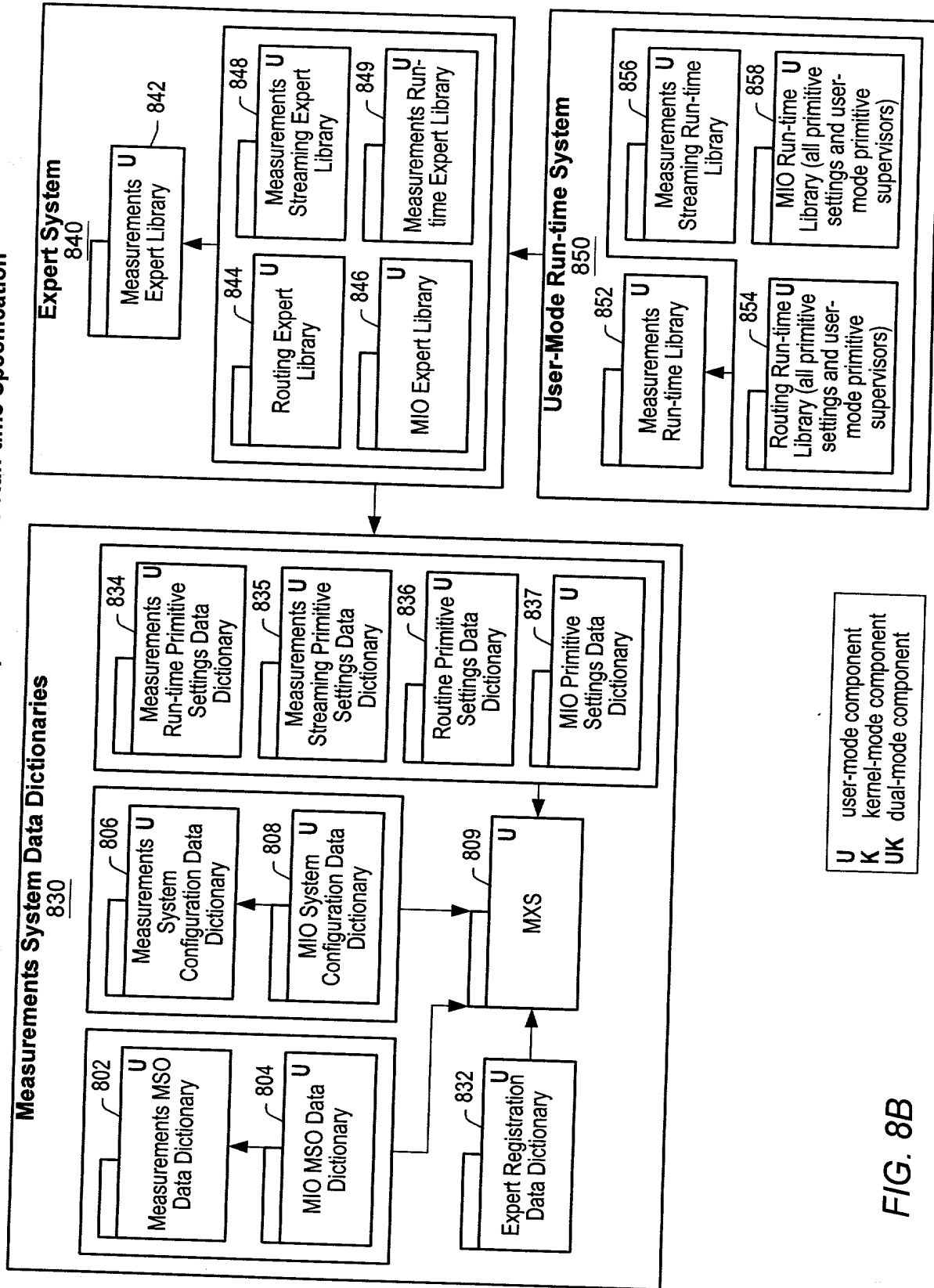


FIG. 8B

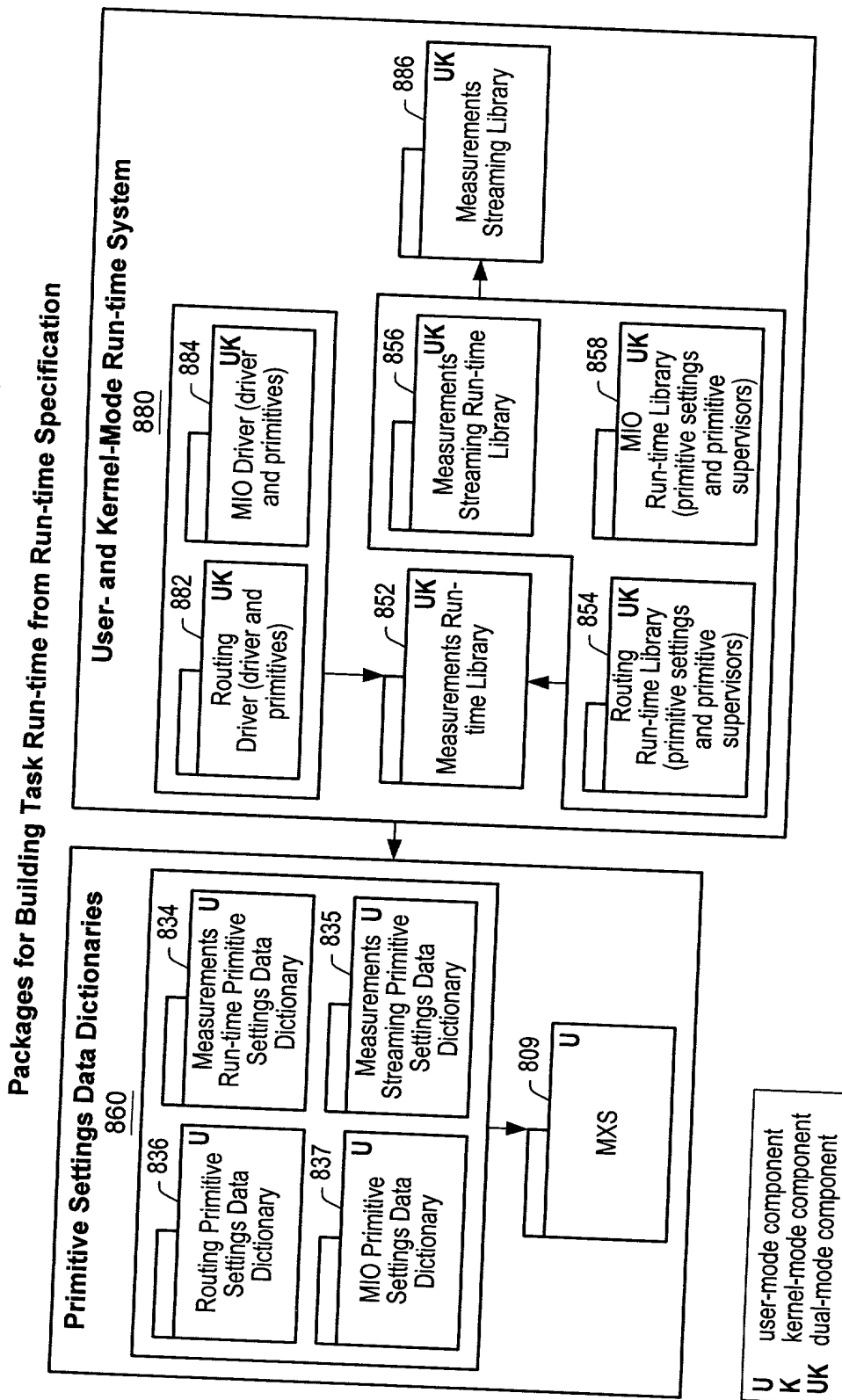


FIG. 8C

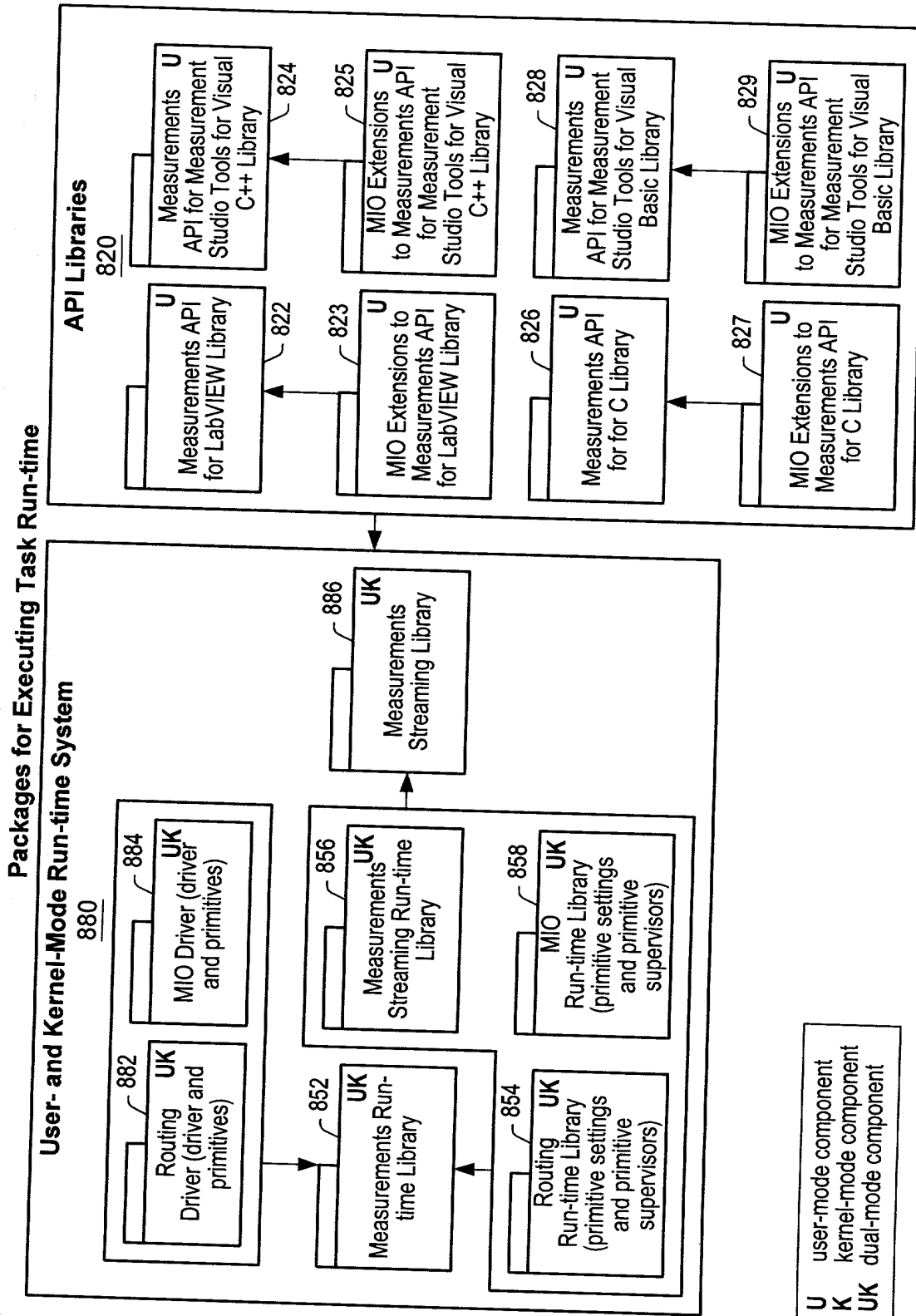


FIG. 8D

State Diagram for Measurement Tasks

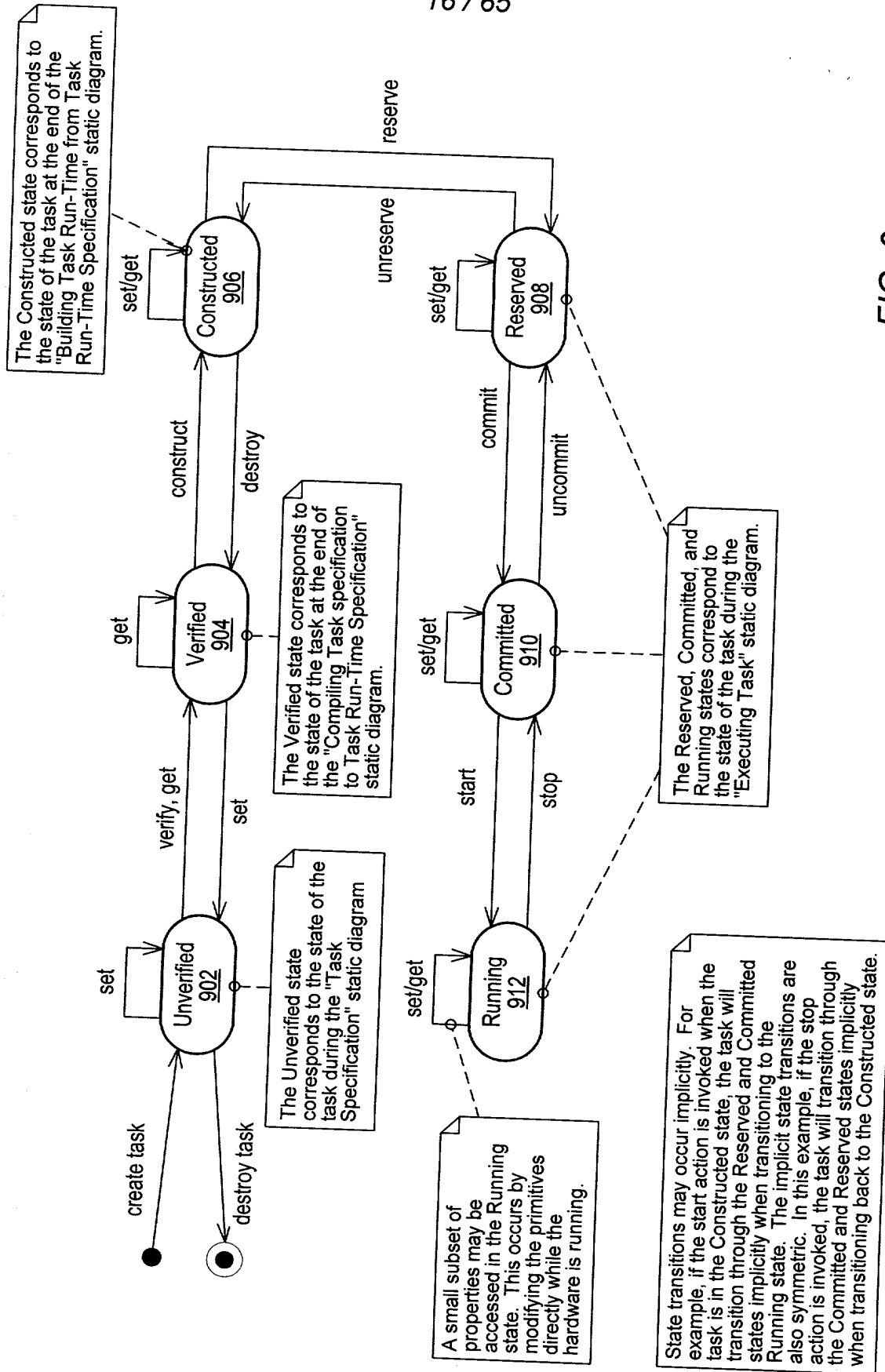


FIG. 9

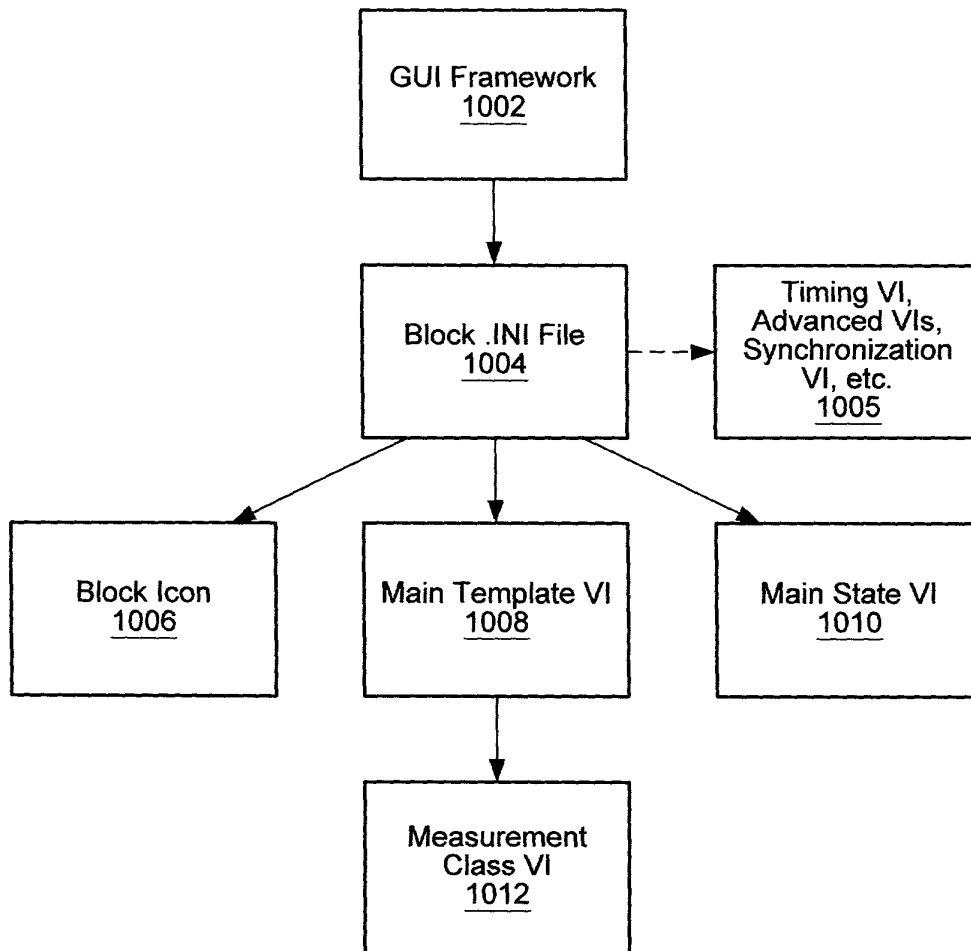


FIG. 10

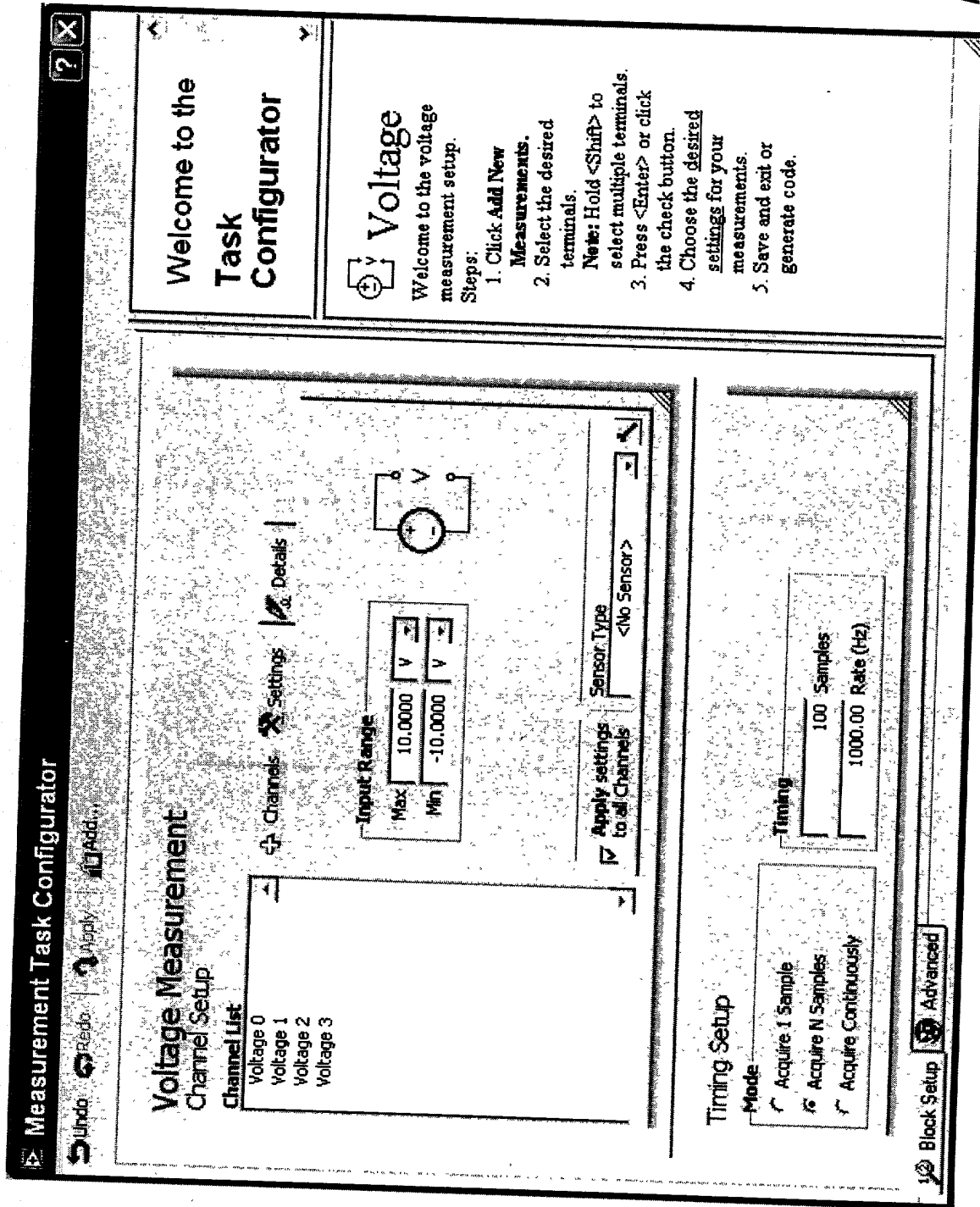


FIG. 11

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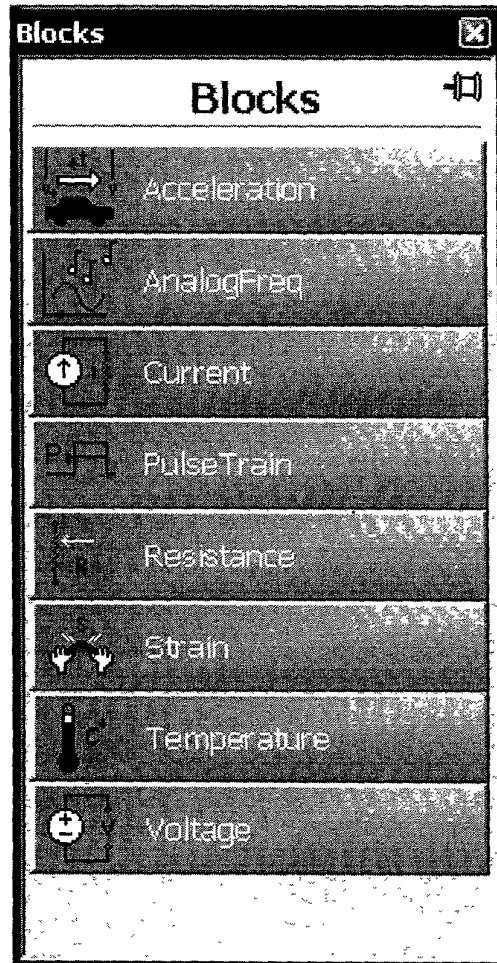


FIG. 12A

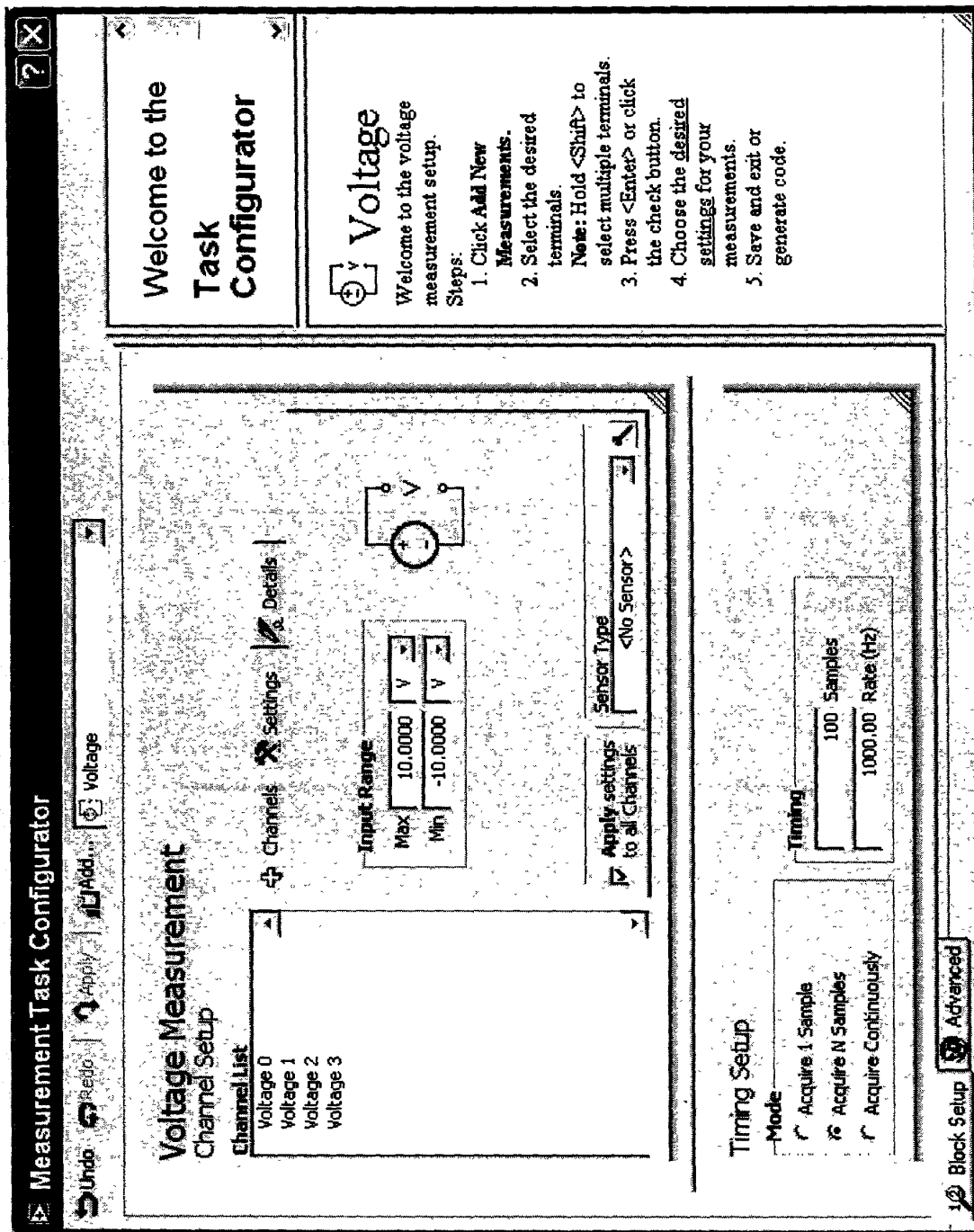


FIG. 12B

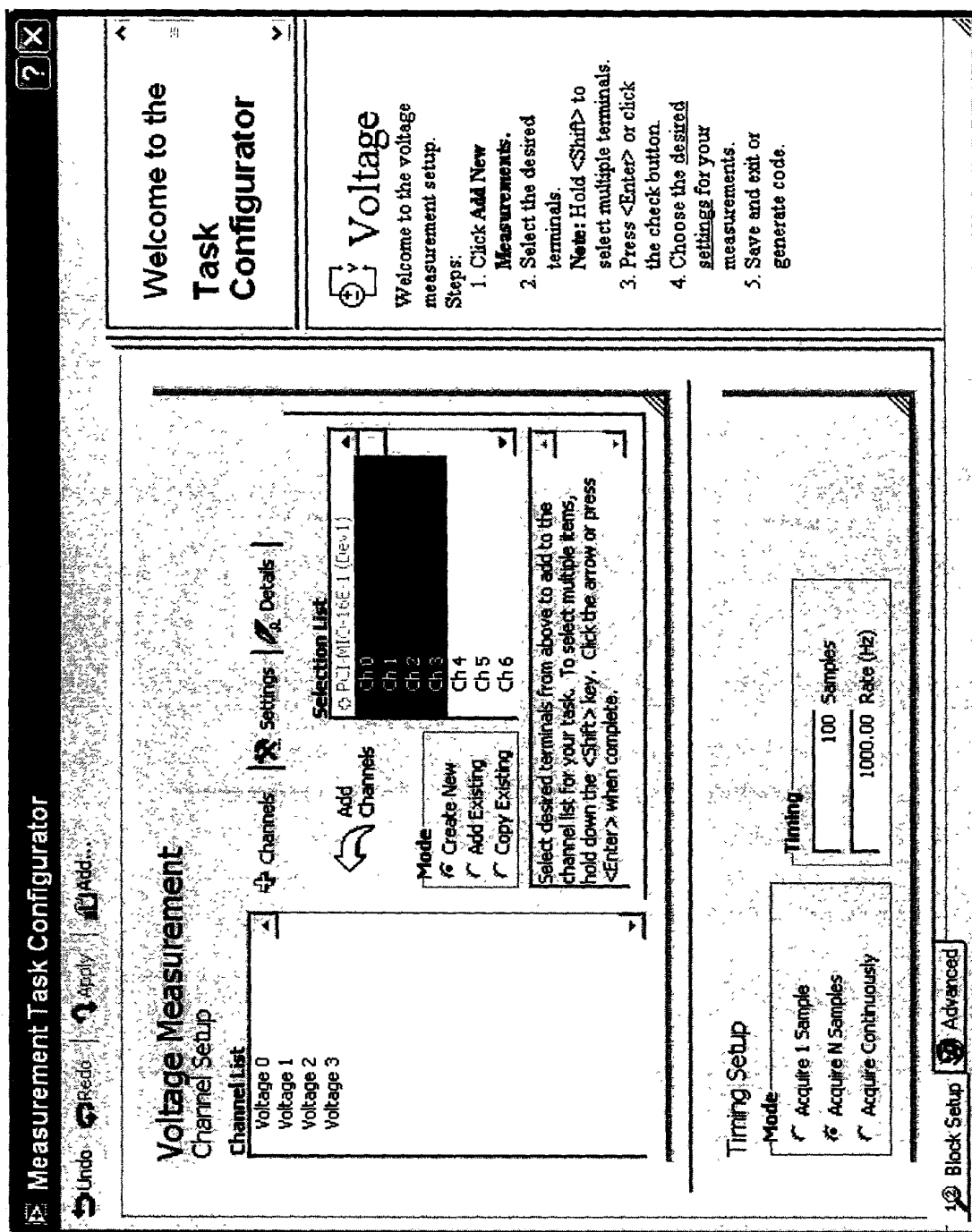


FIG. 12C

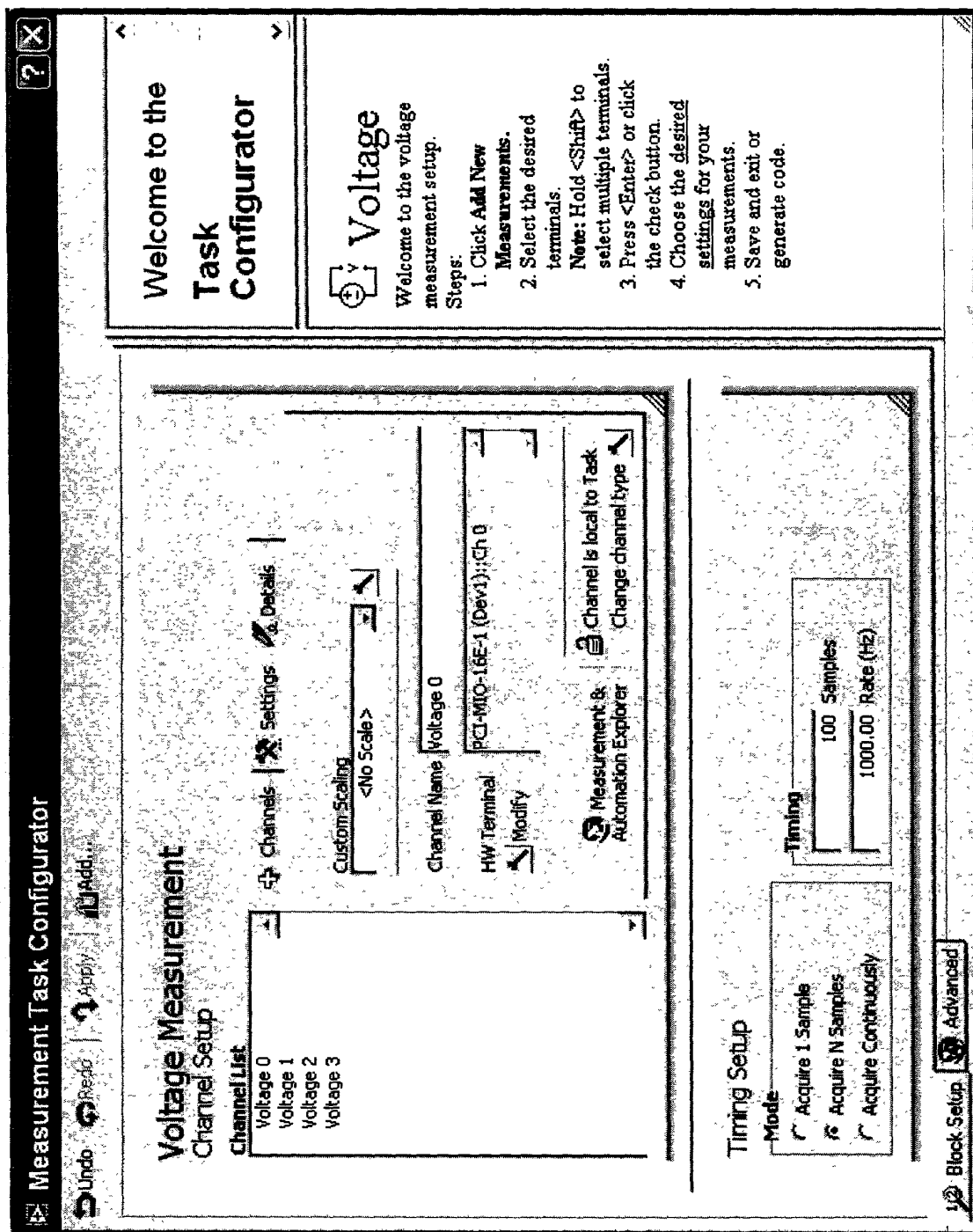


FIG. 12D

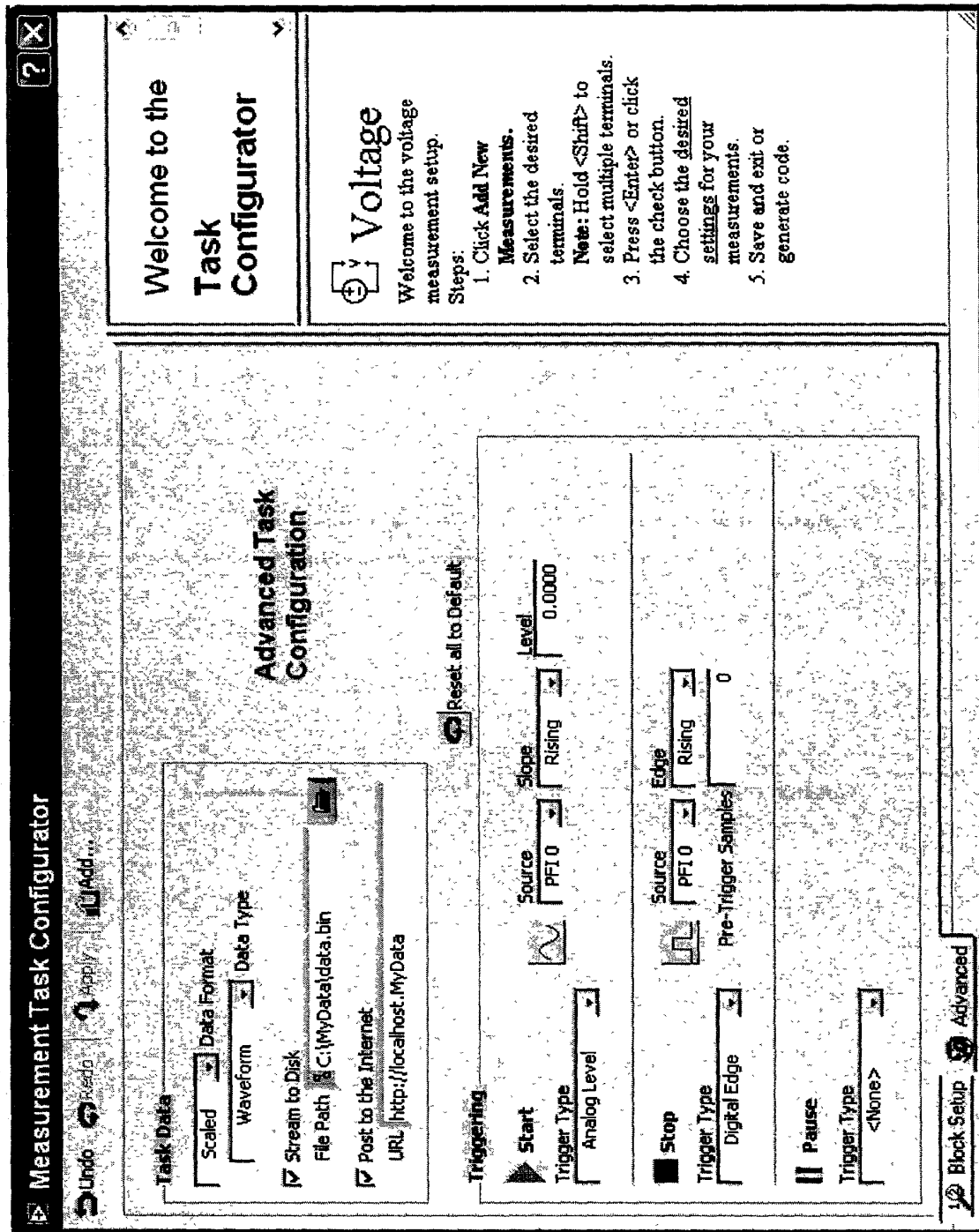


FIG. 13

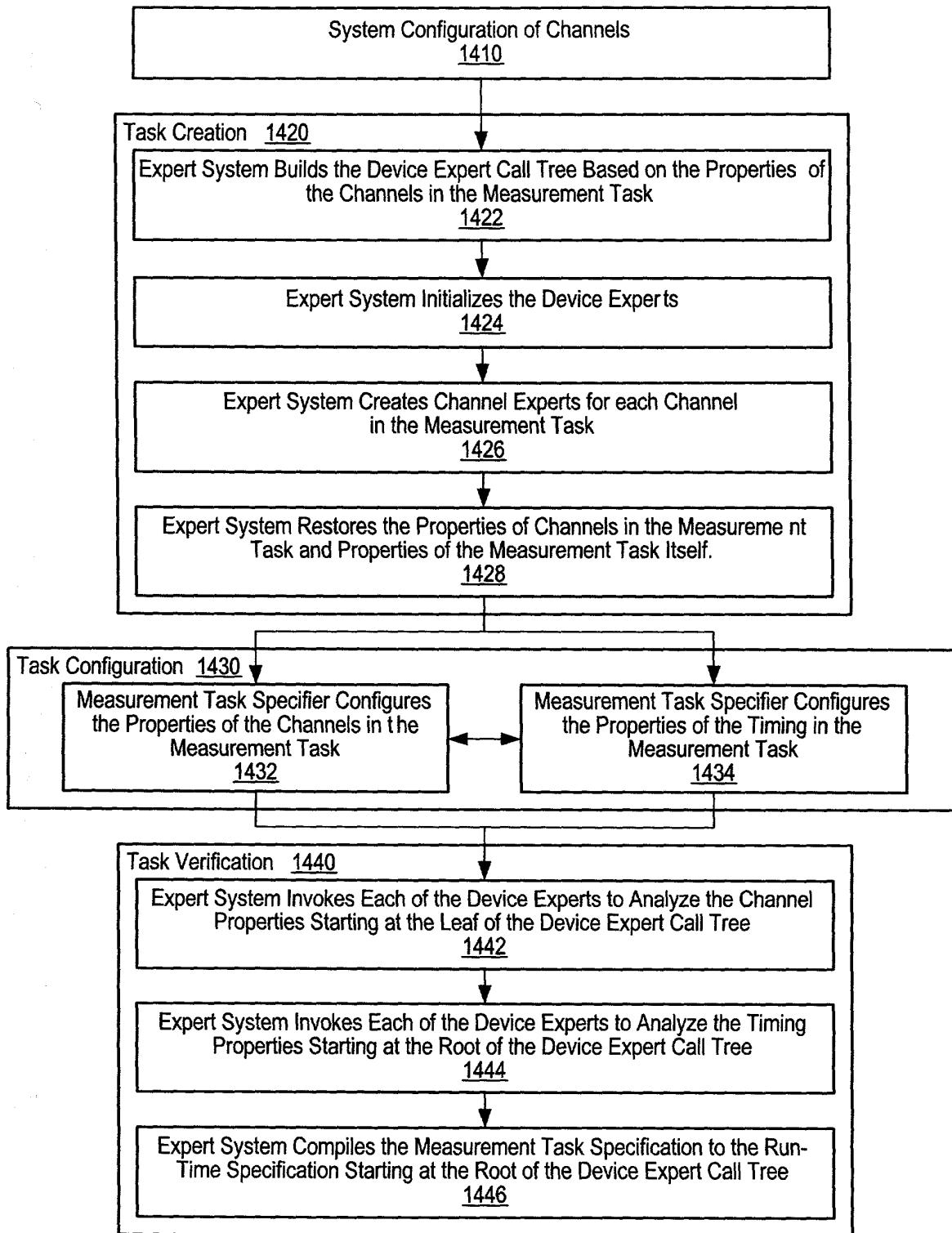


FIG. 14

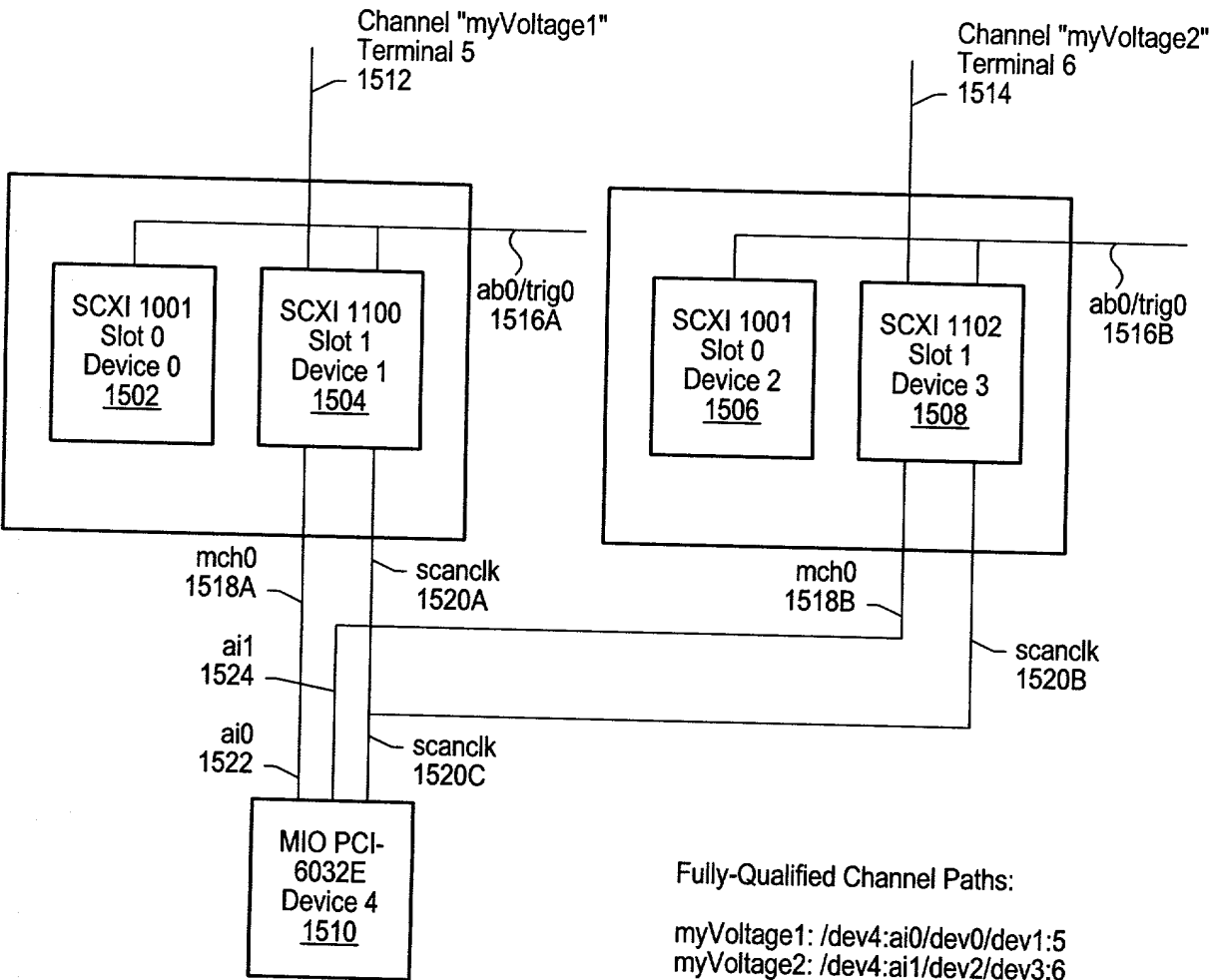


FIG. 15

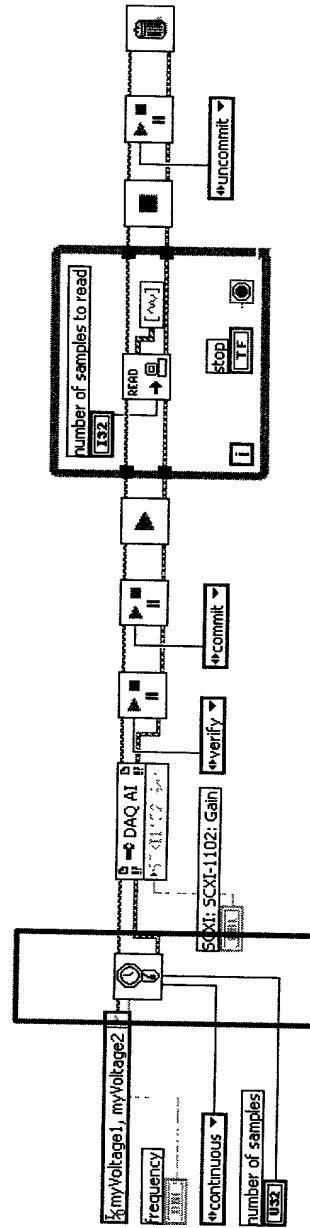
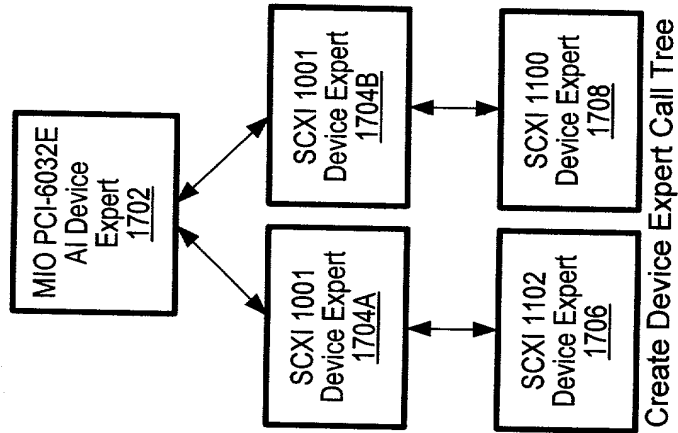
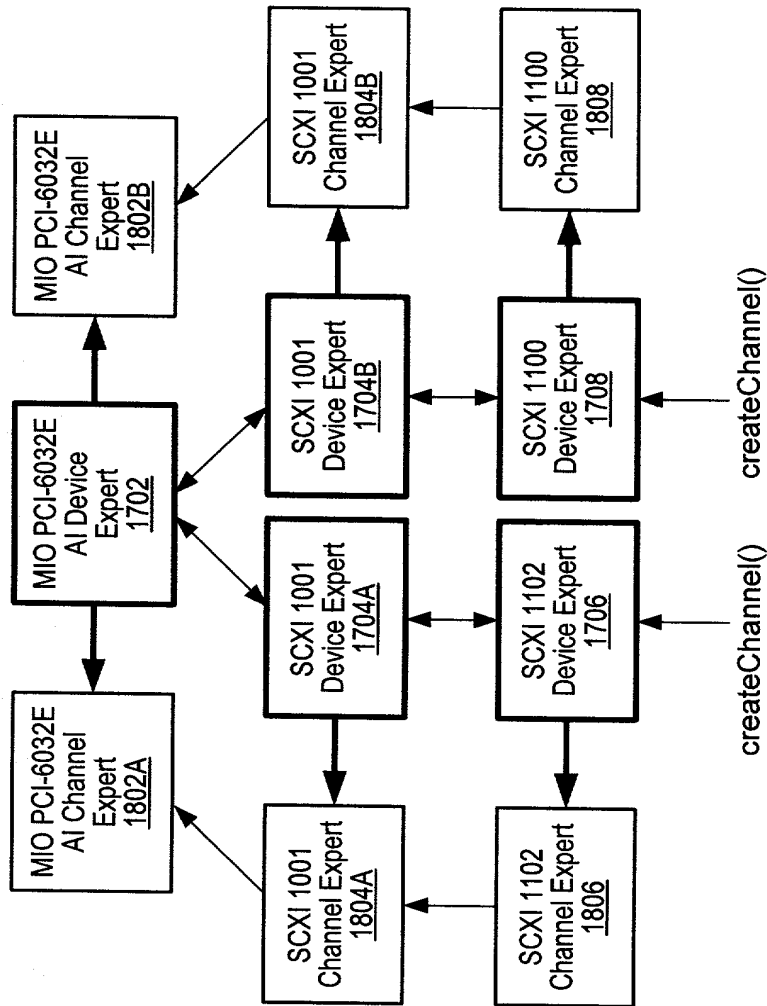


FIG. 17



createChannel() Create Channel Experts

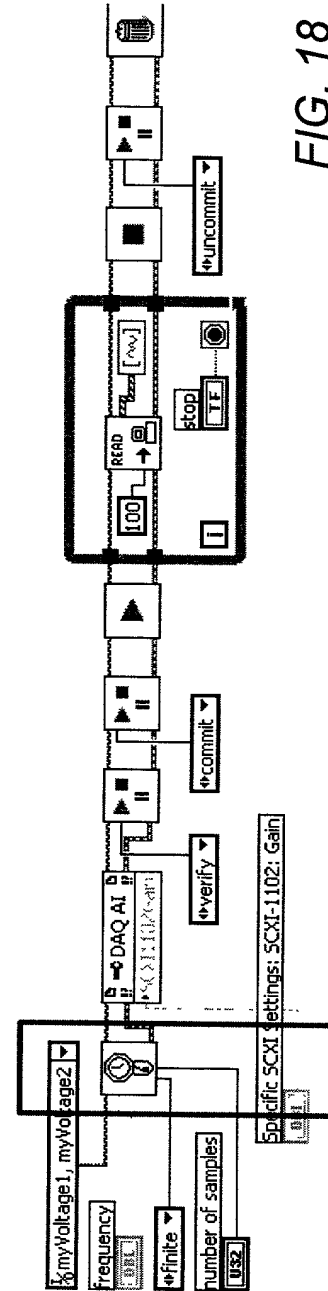
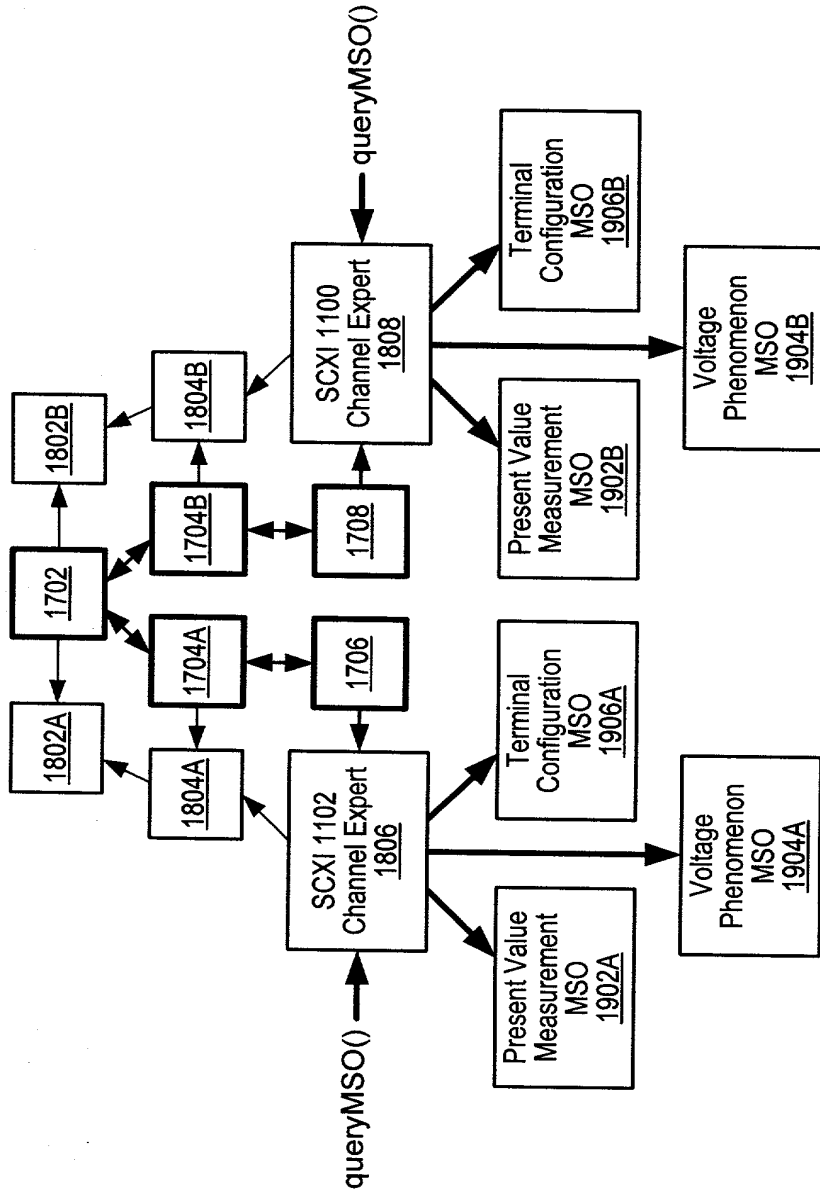


FIG. 18



Deserialize Named Channel MSOs

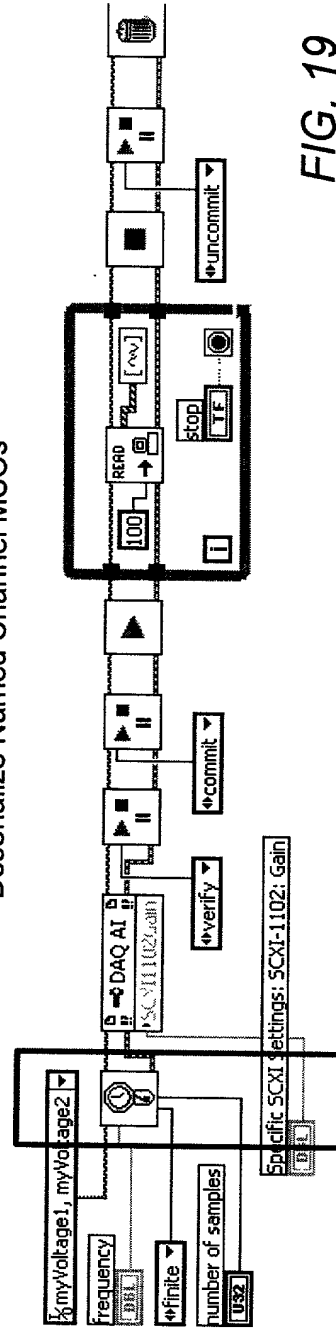


FIG. 19

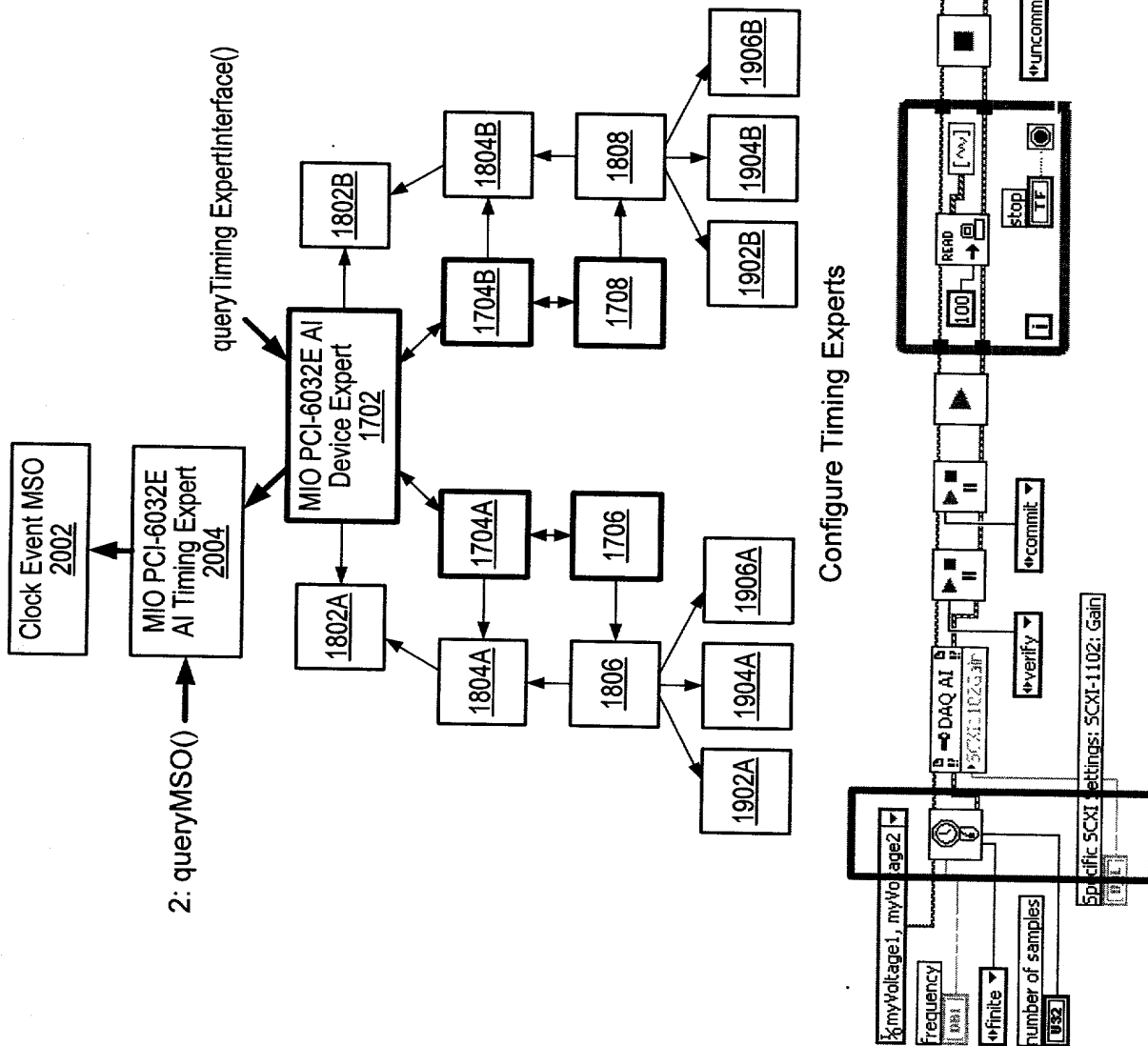


FIG. 20

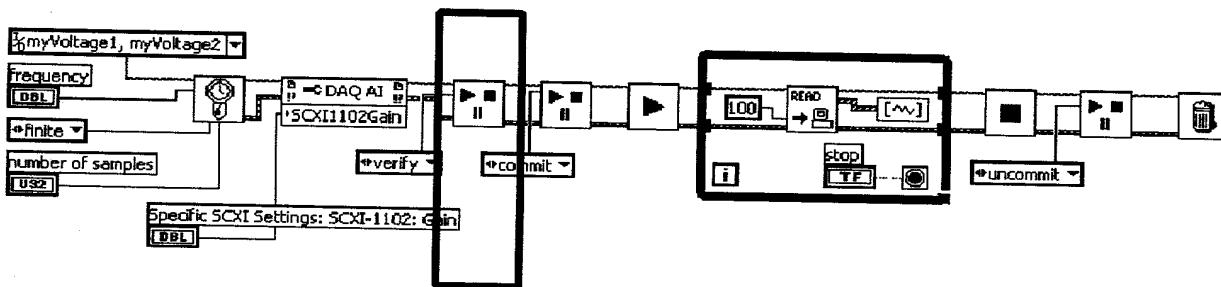
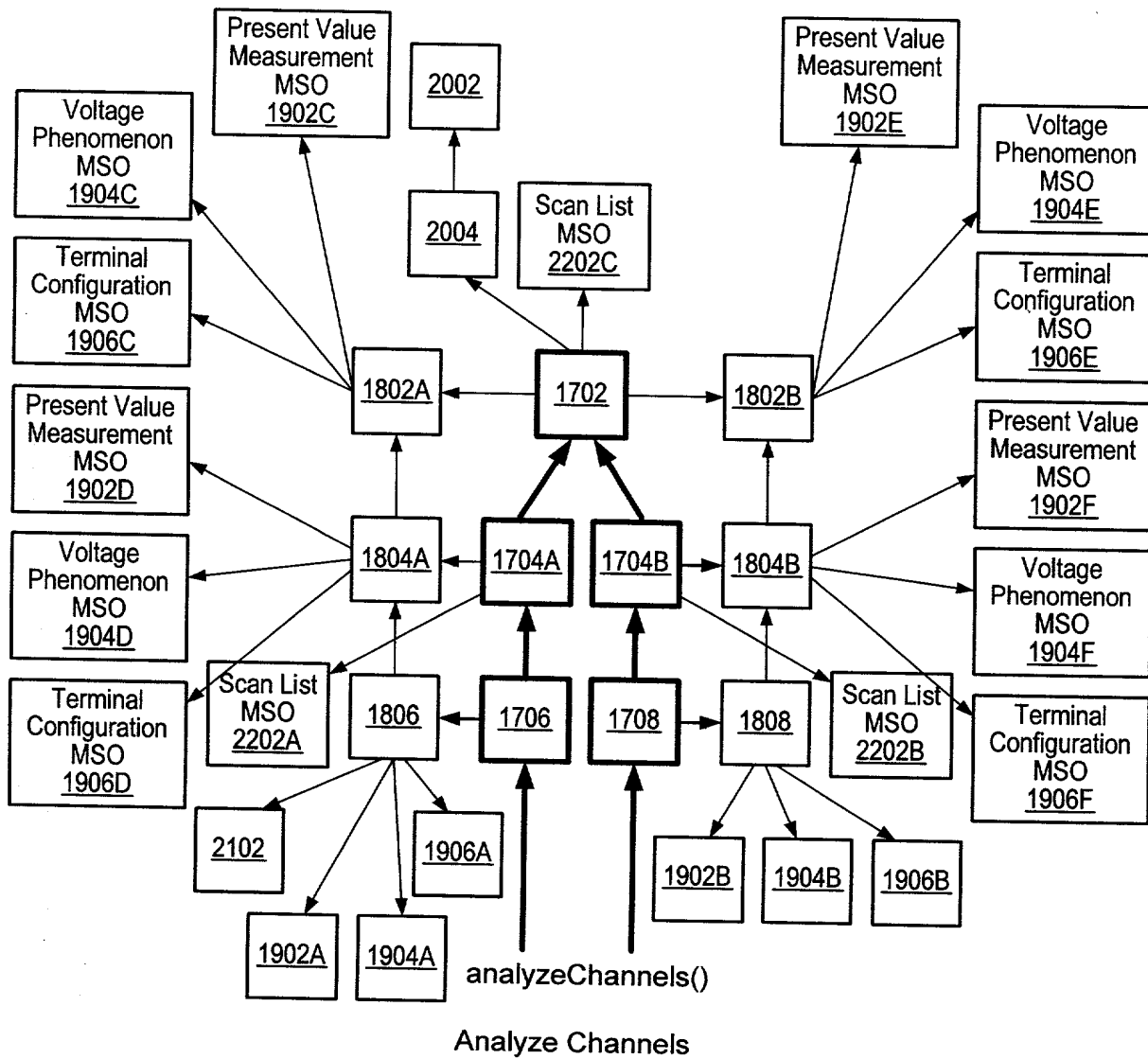
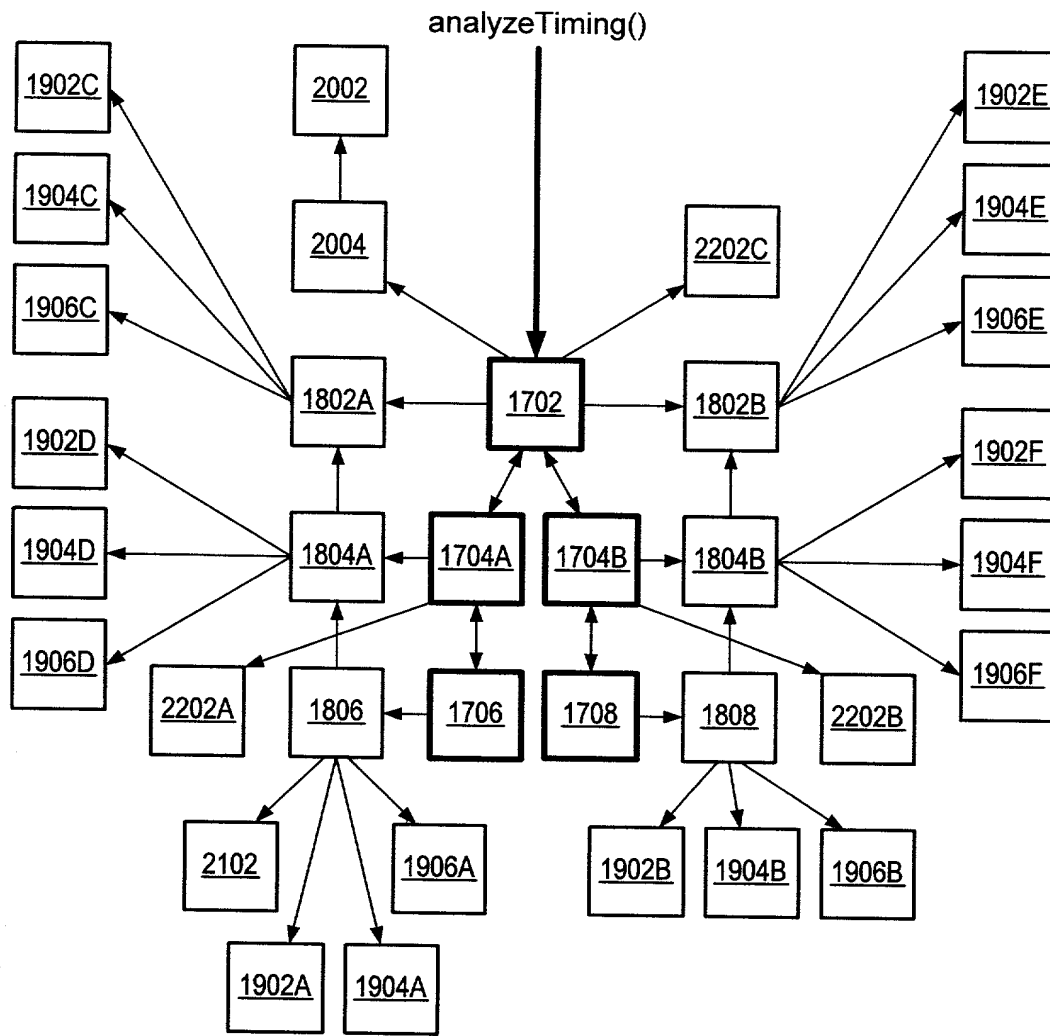


FIG. 22



Analyze Timing

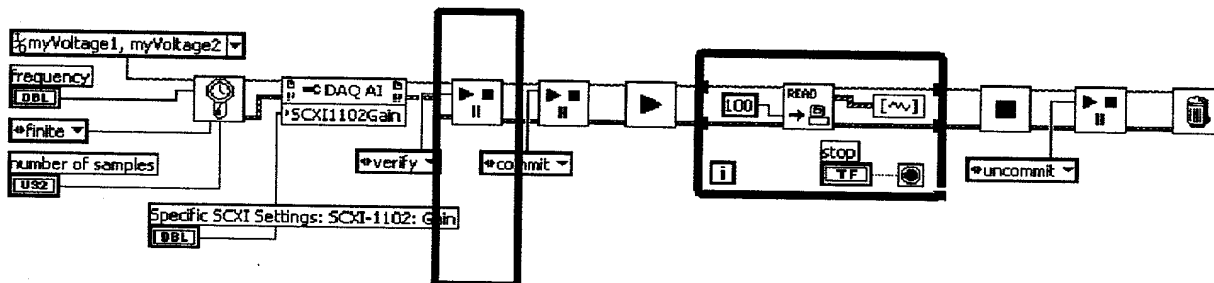


FIG. 23

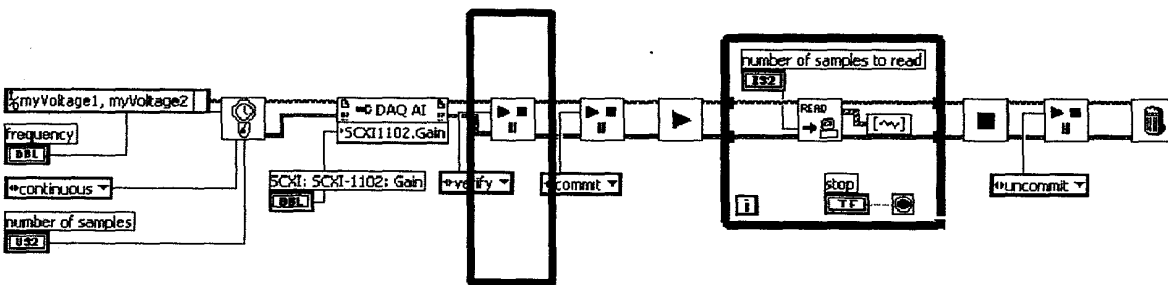
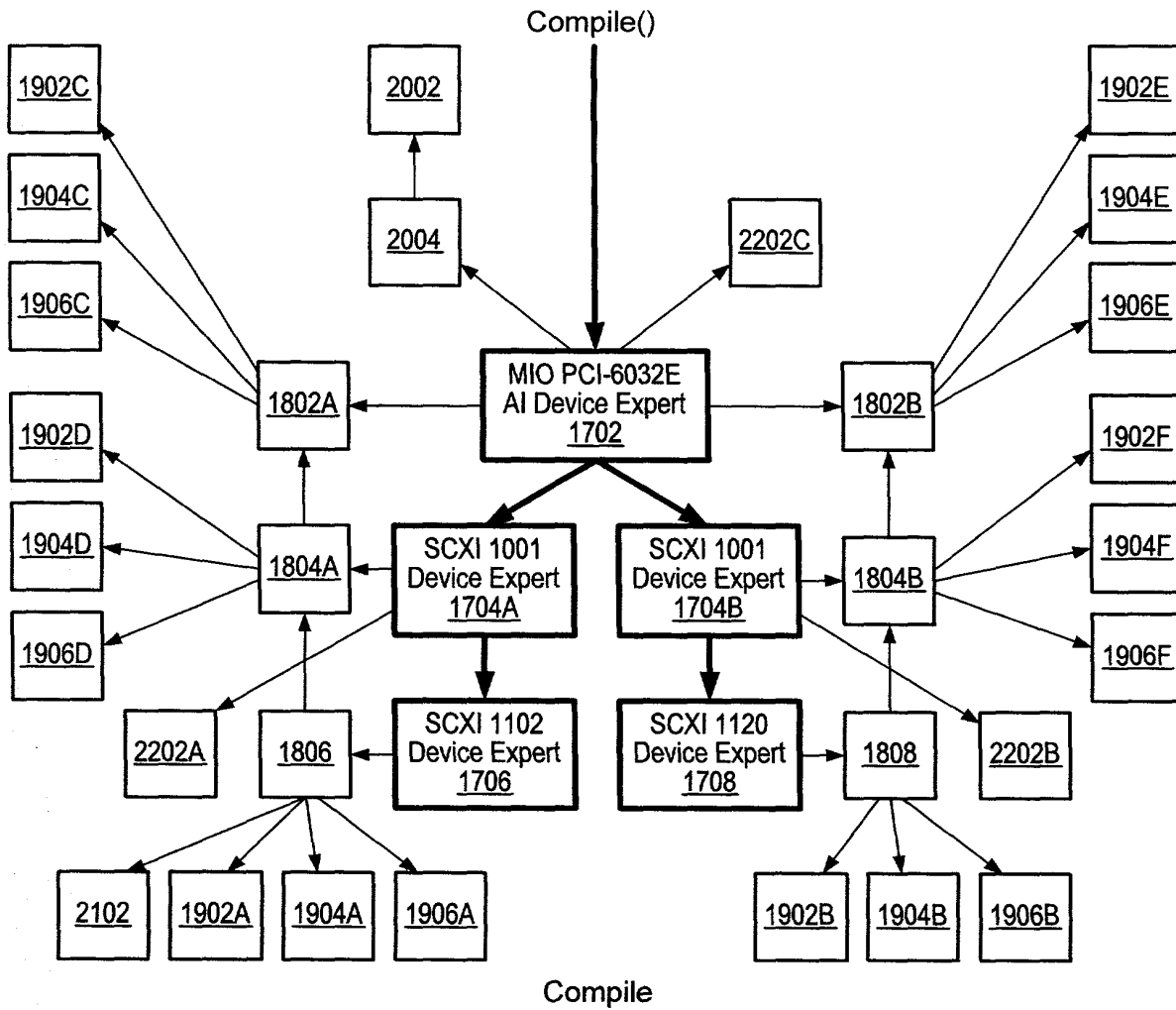


FIG. 24A

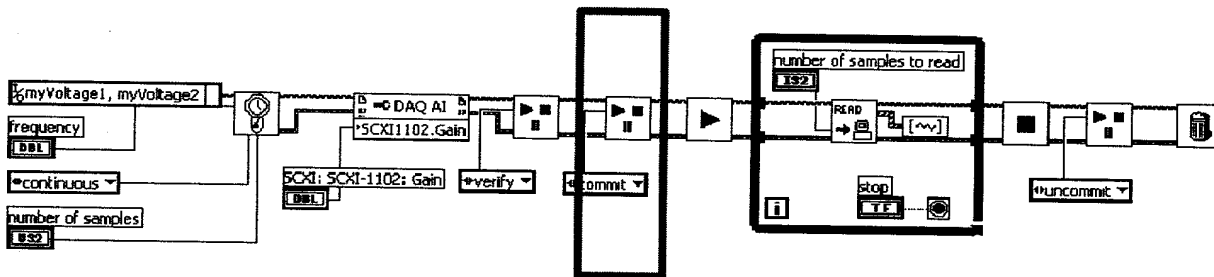
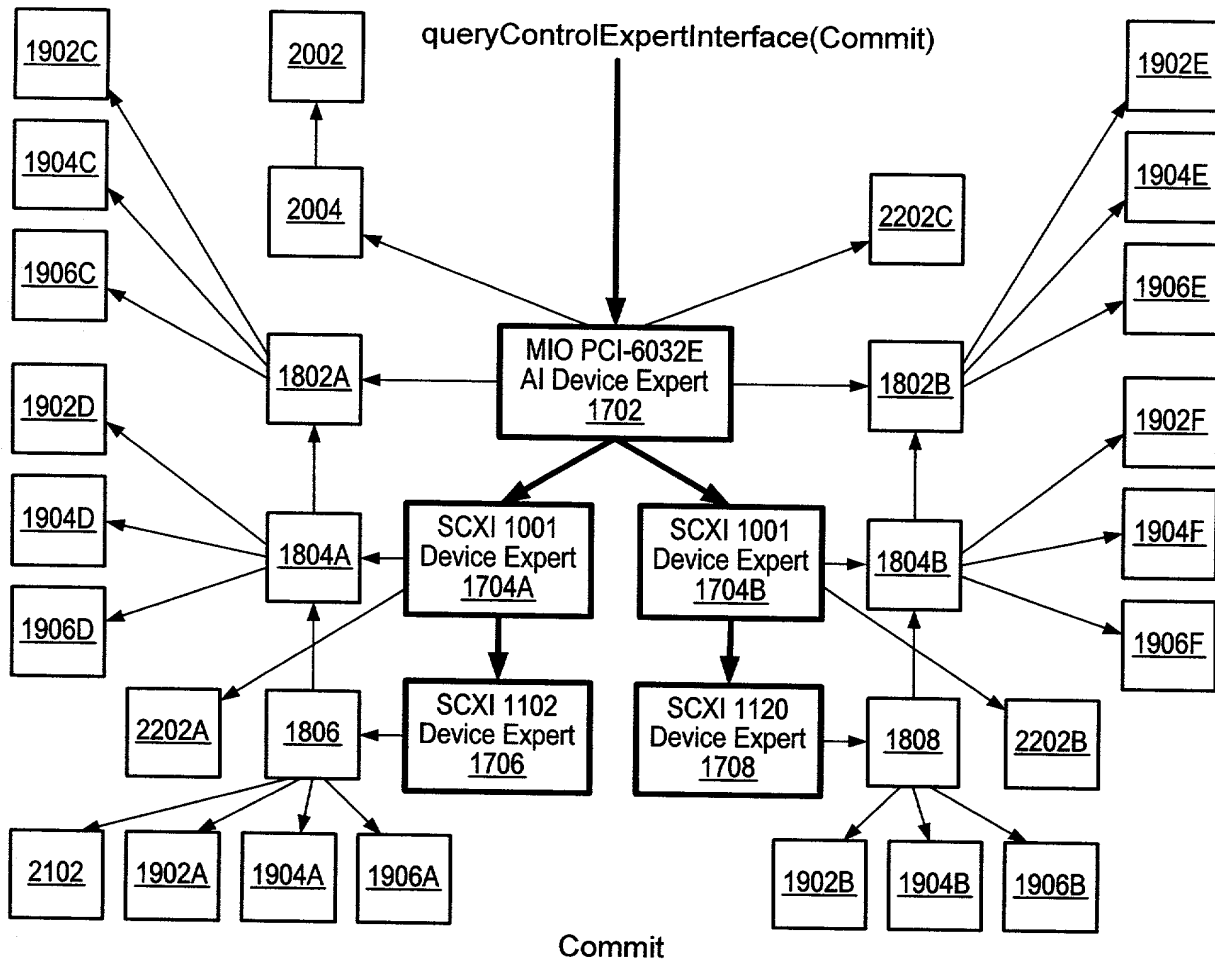


FIG. 24B

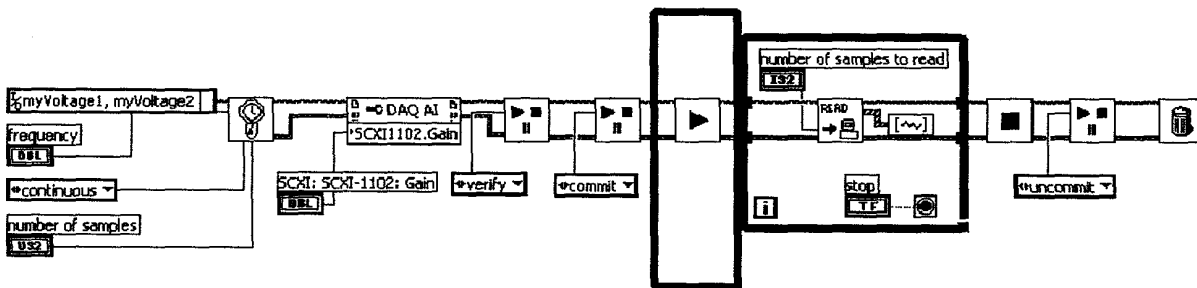
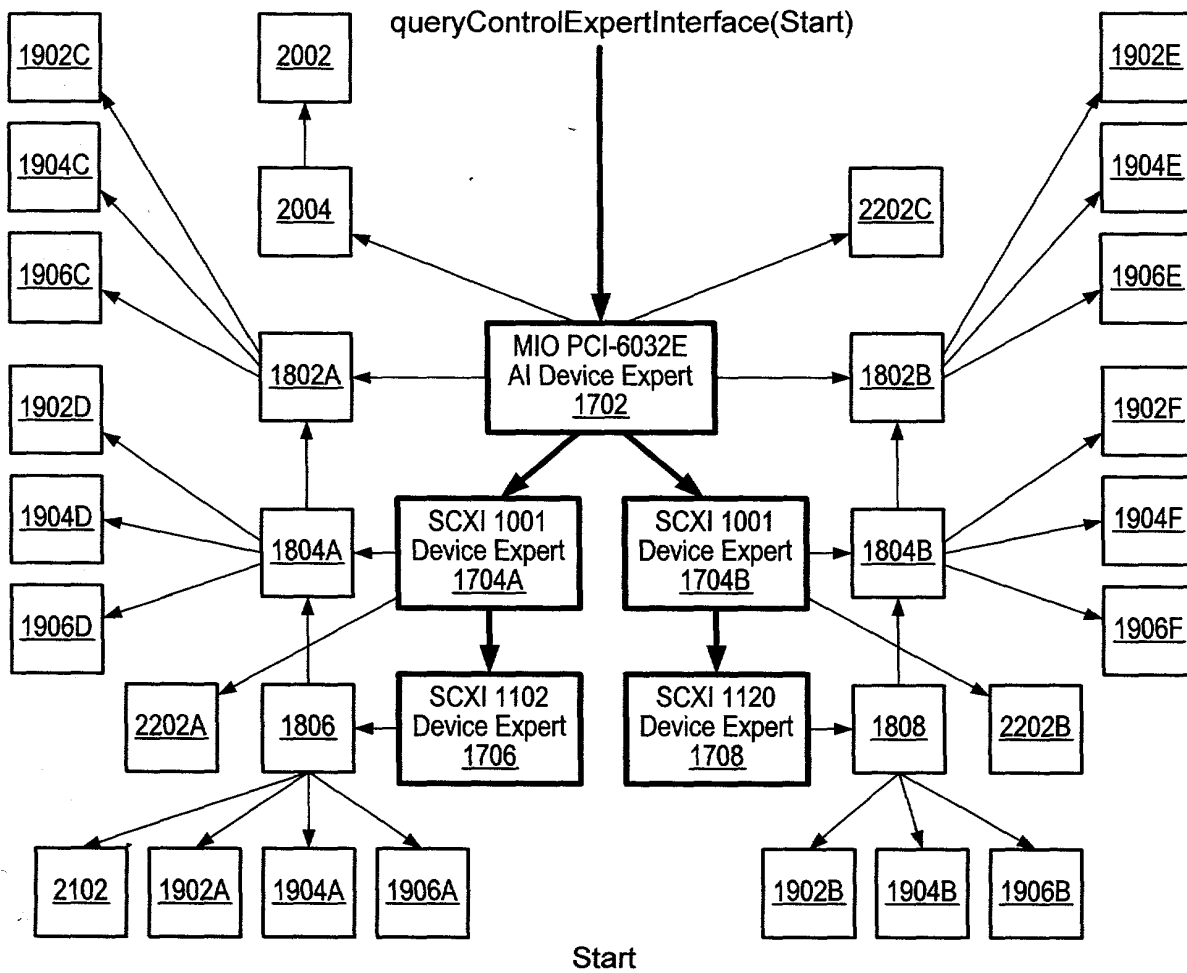


FIG. 24C

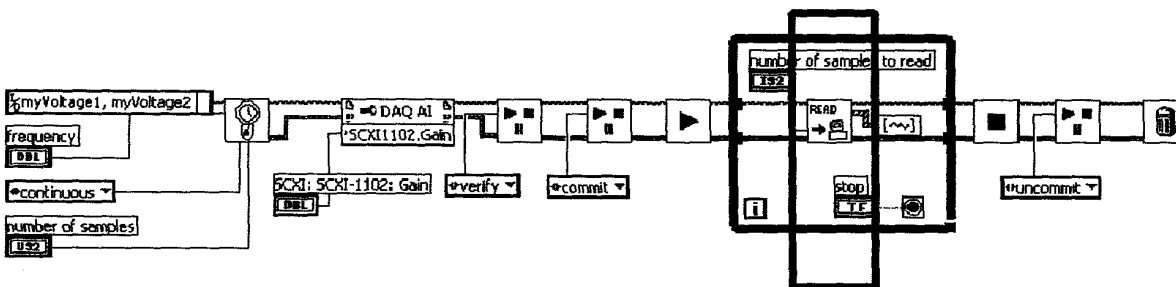
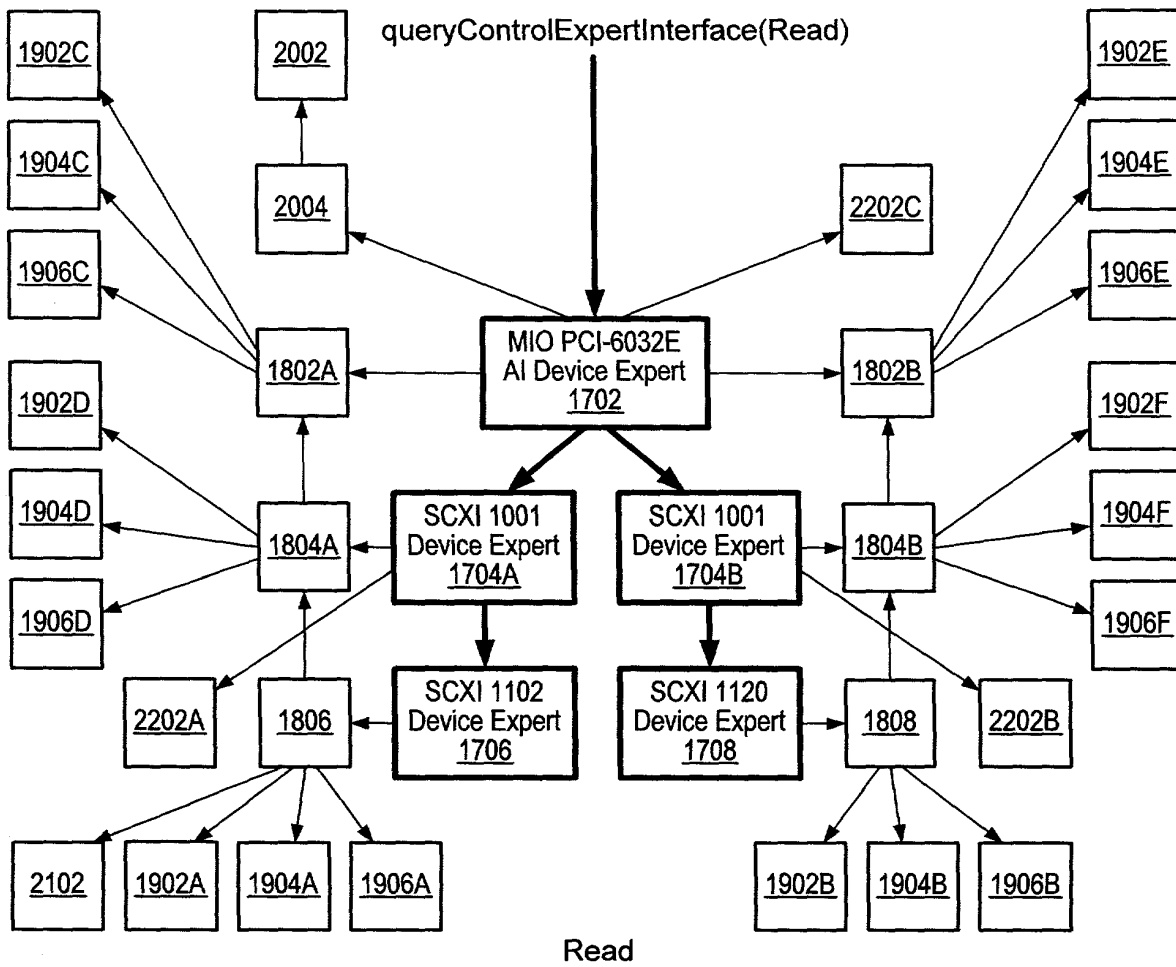


FIG. 24D

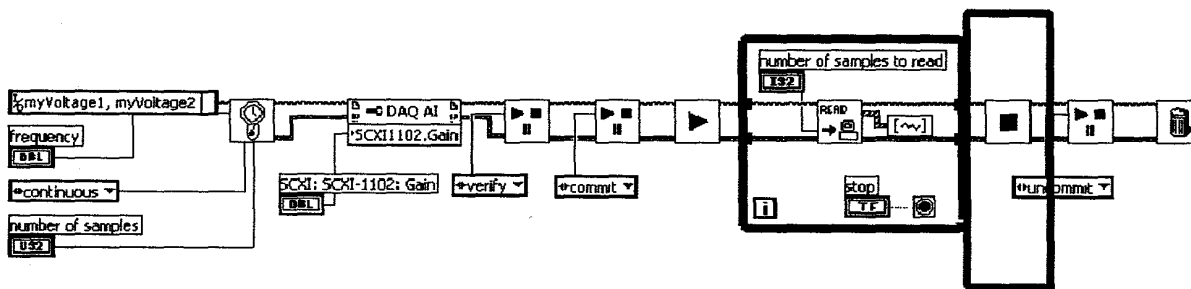
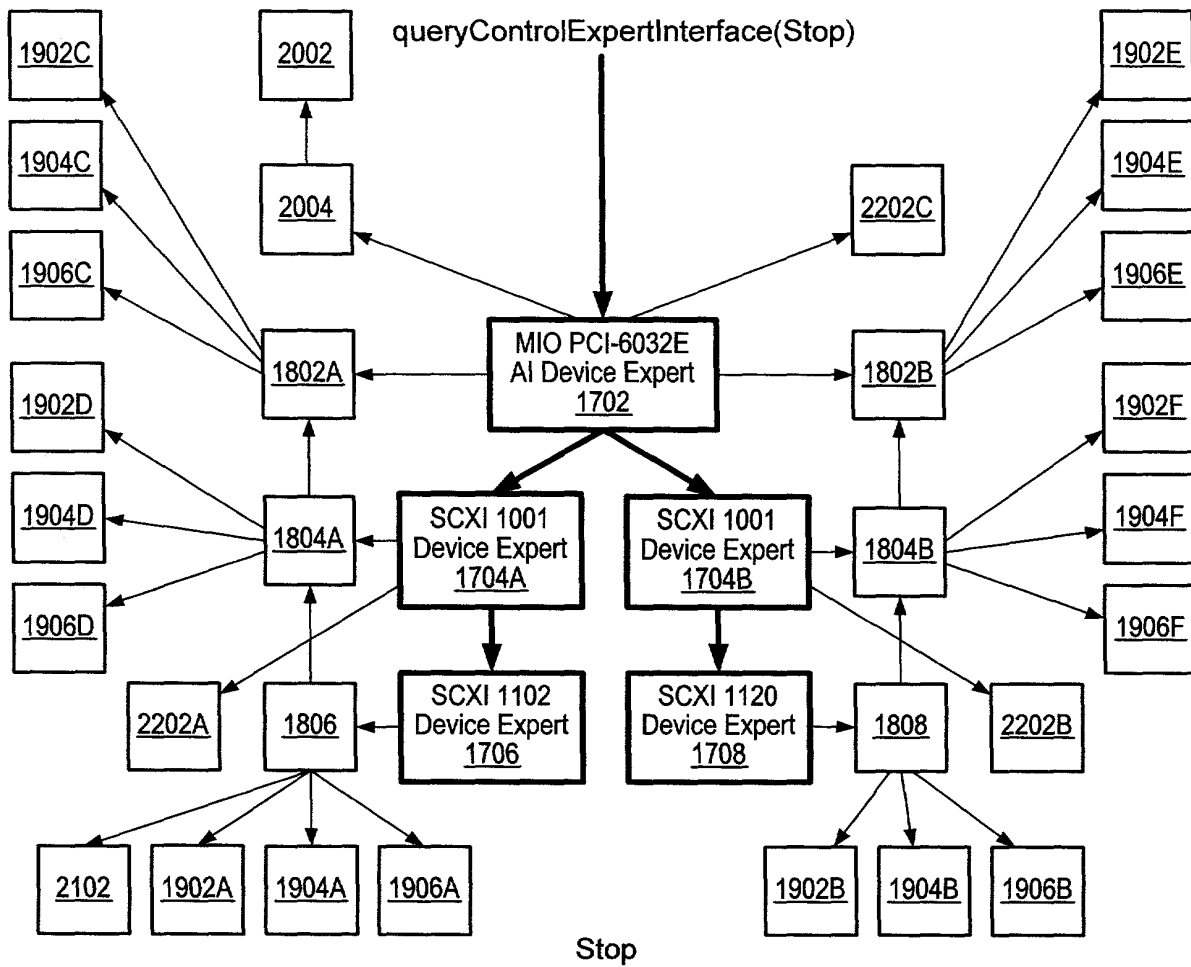


FIG. 24E

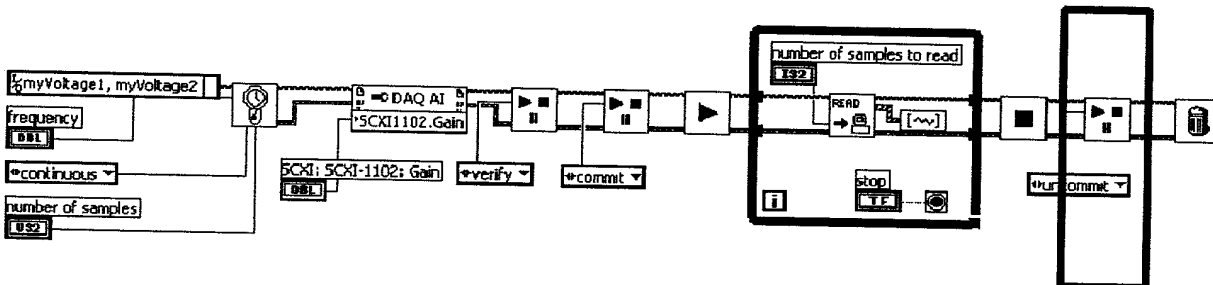
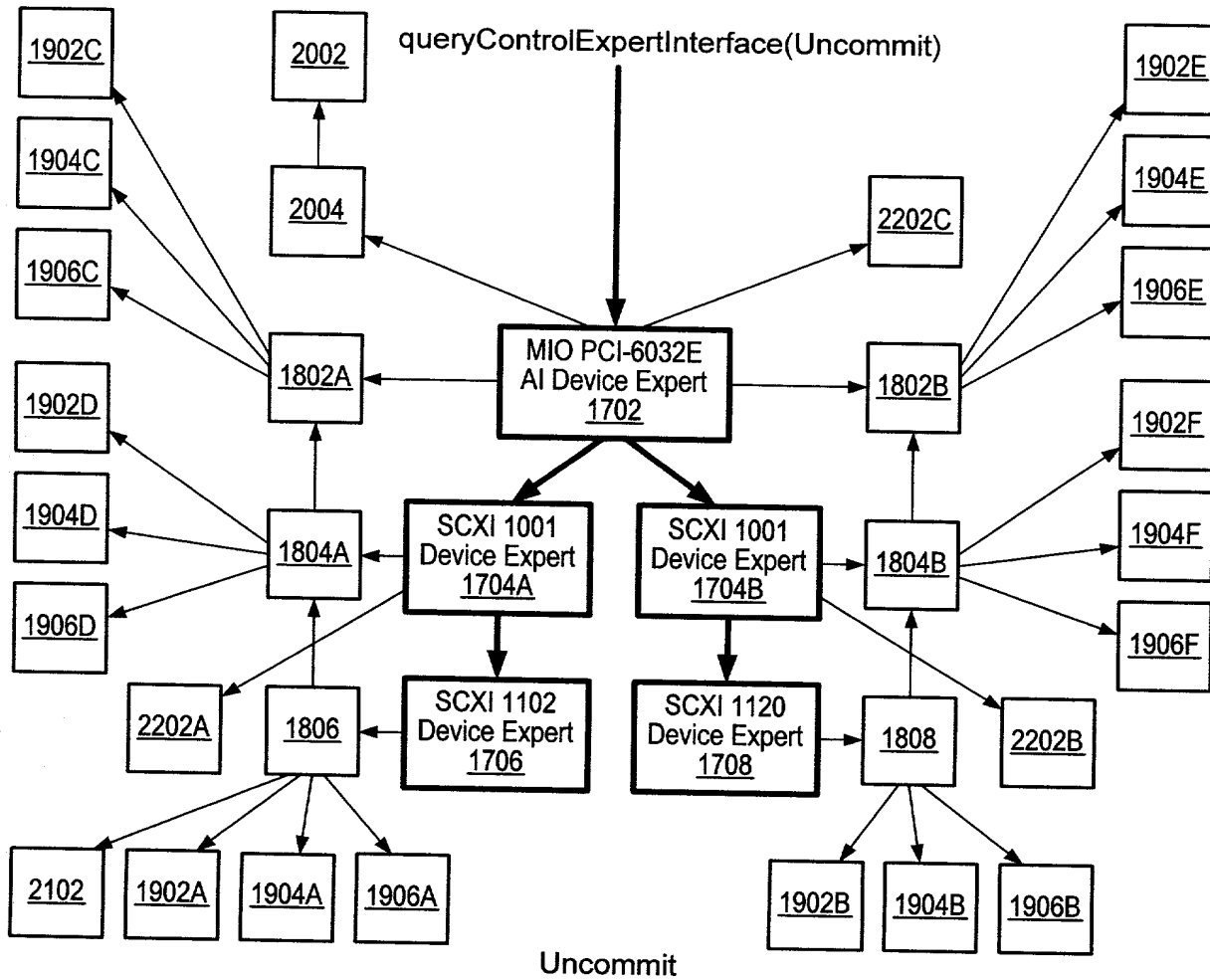
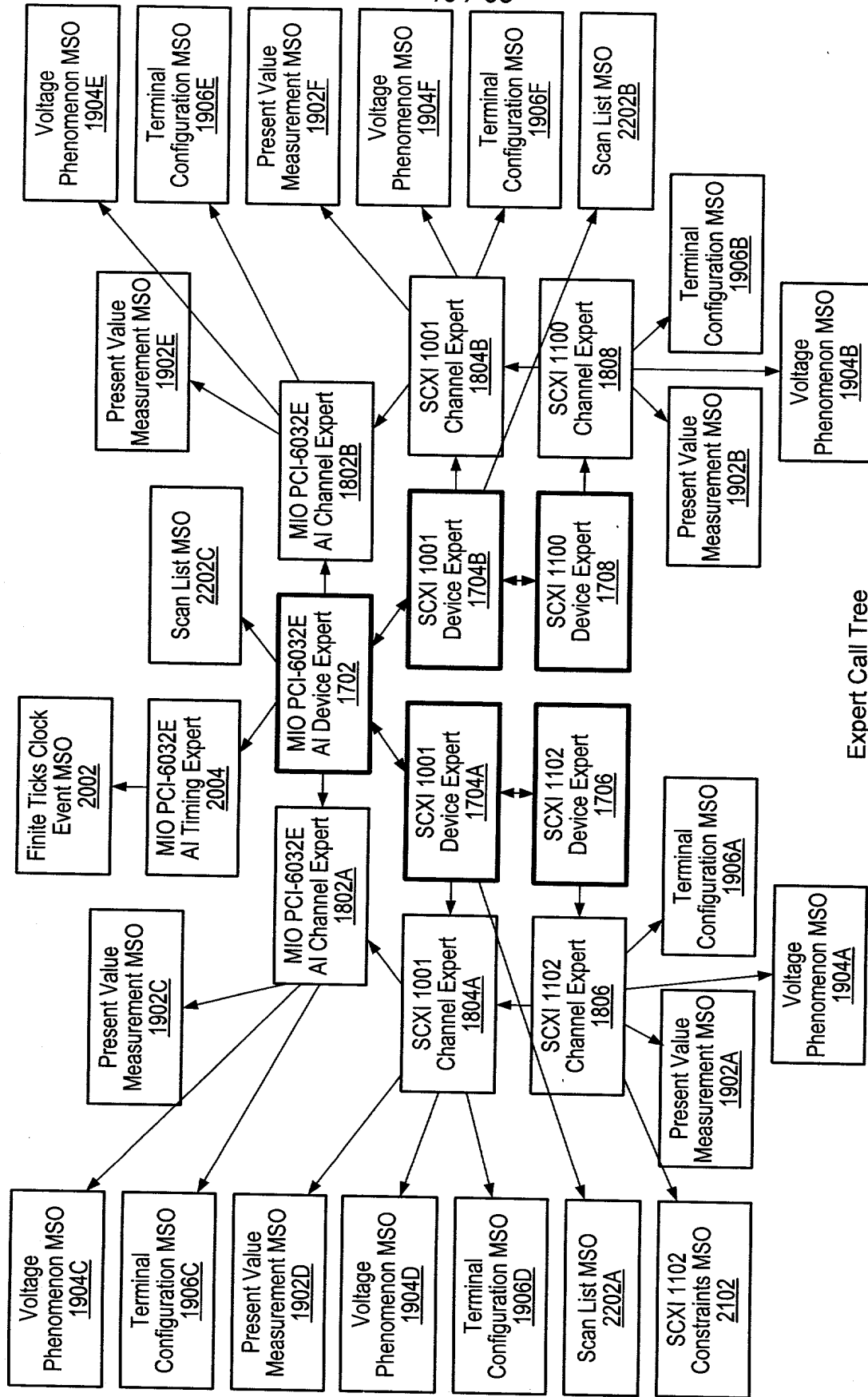


FIG. 24F



Expert Call Tree

Use Case: Multi-Chassis SCXI Finite Acquisition Using An MIO

FIG. 25

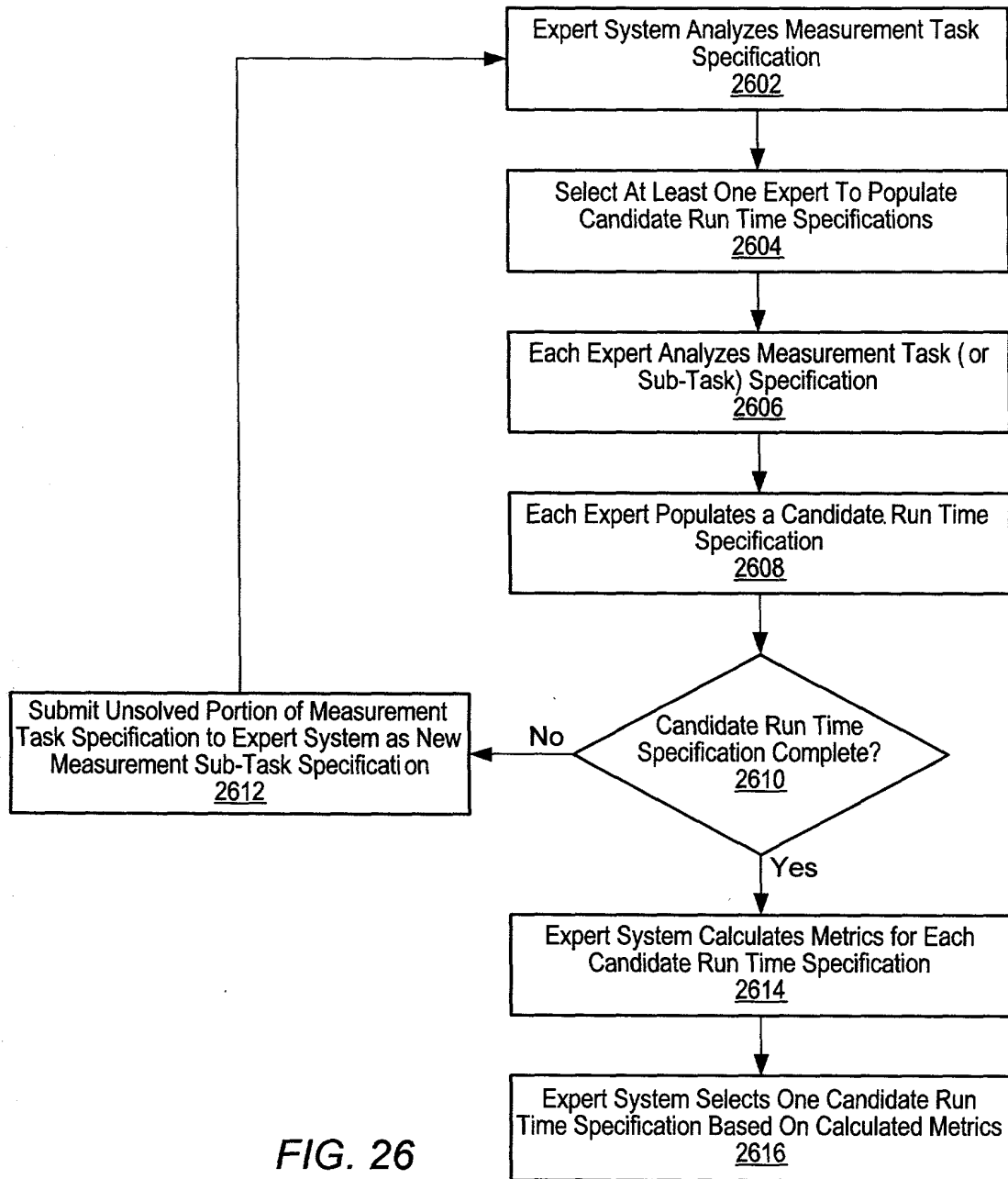


FIG. 26

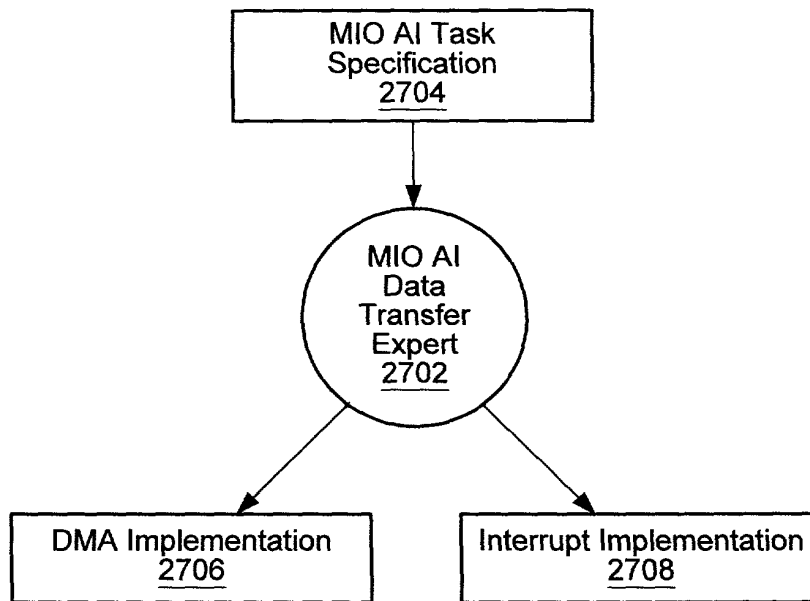


FIG. 27

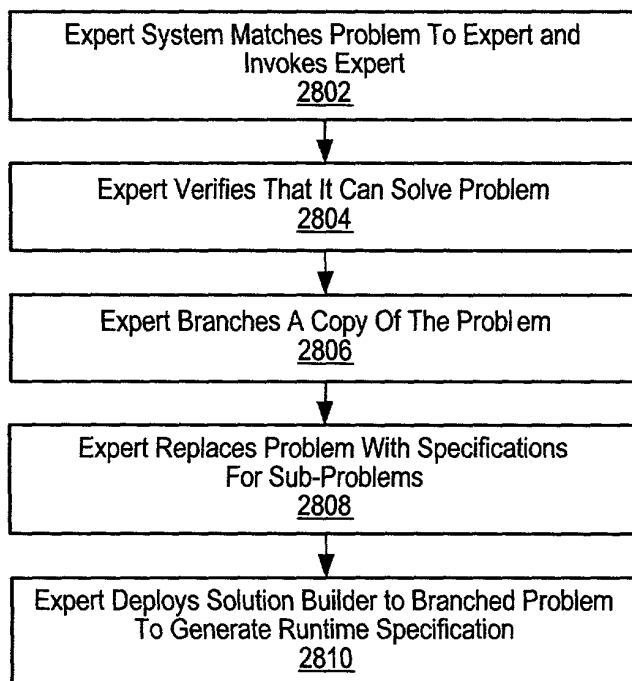


FIG. 28

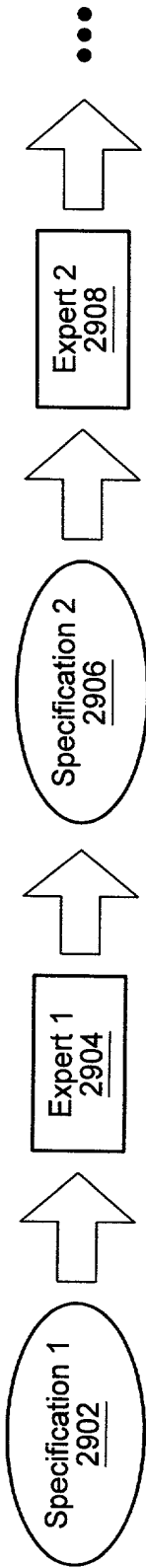


FIG. 29

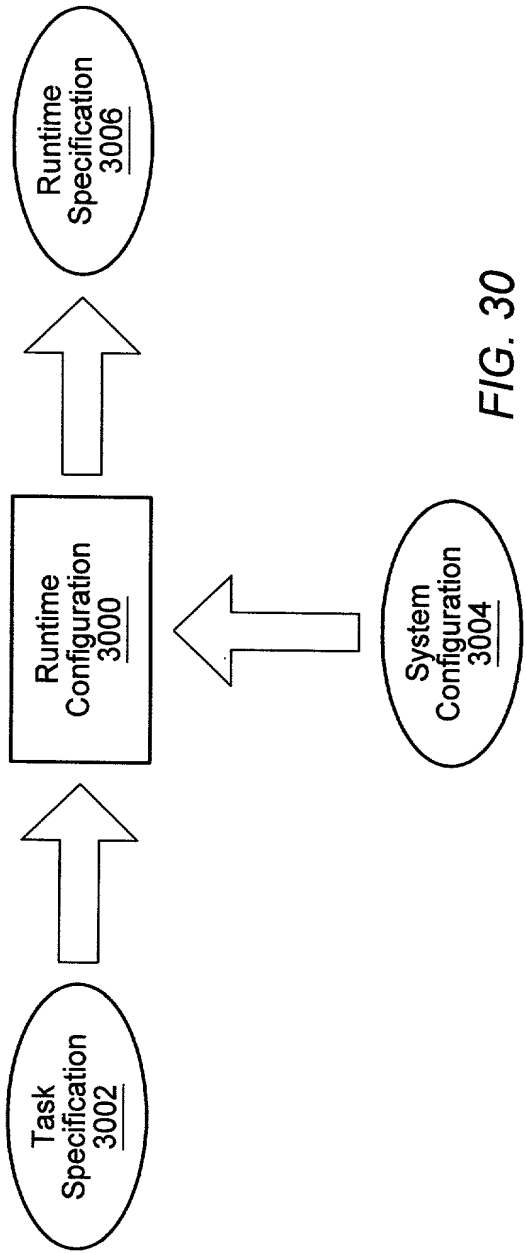


FIG. 30

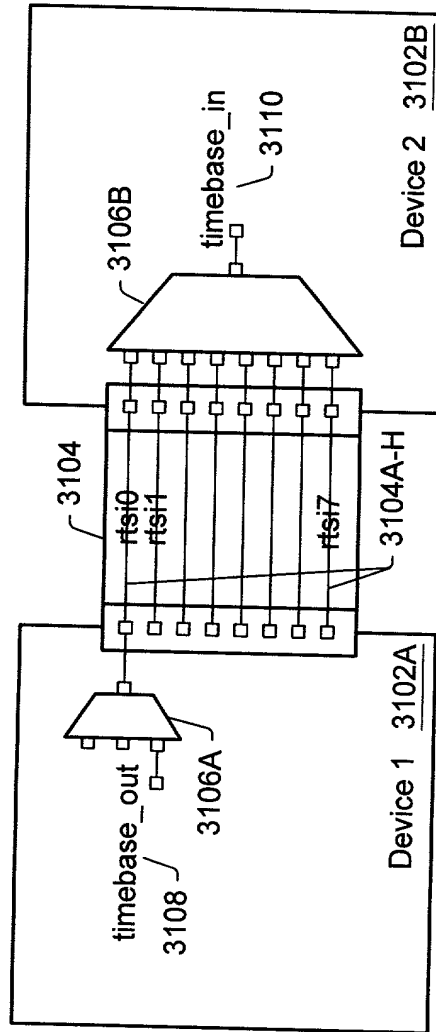


FIG. 31

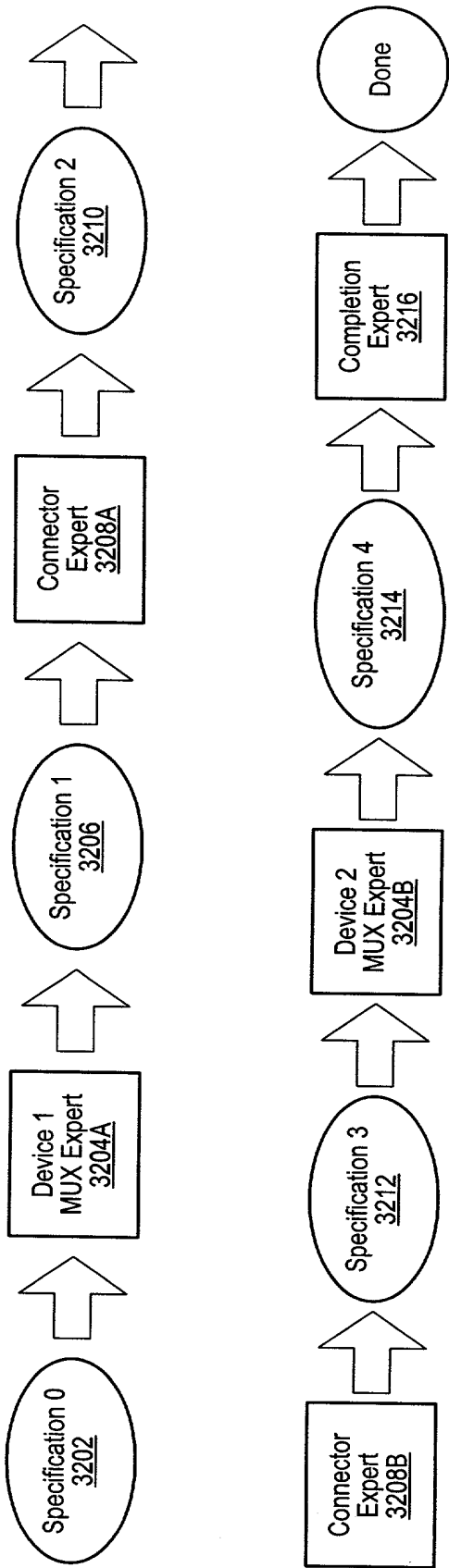


FIG. 32

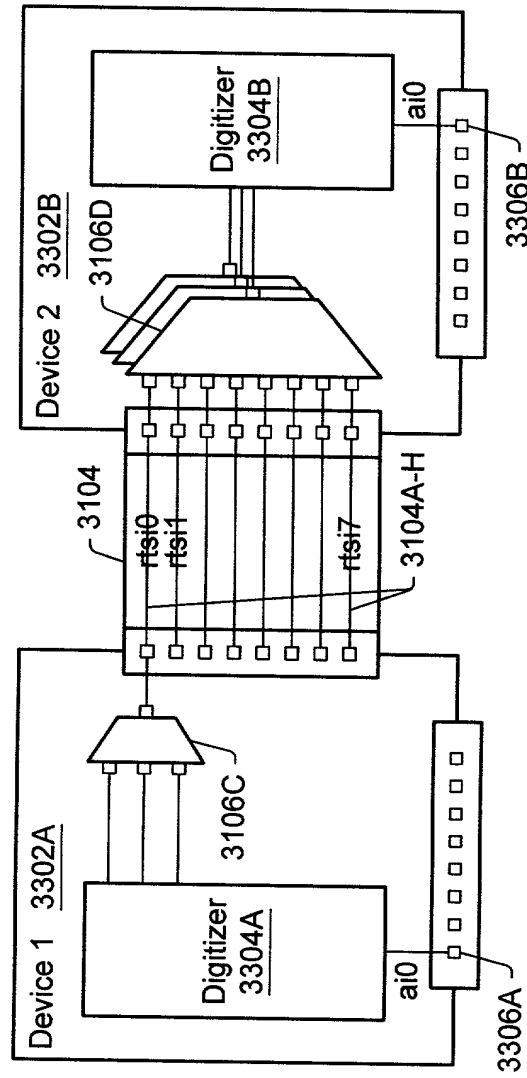


FIG. 33

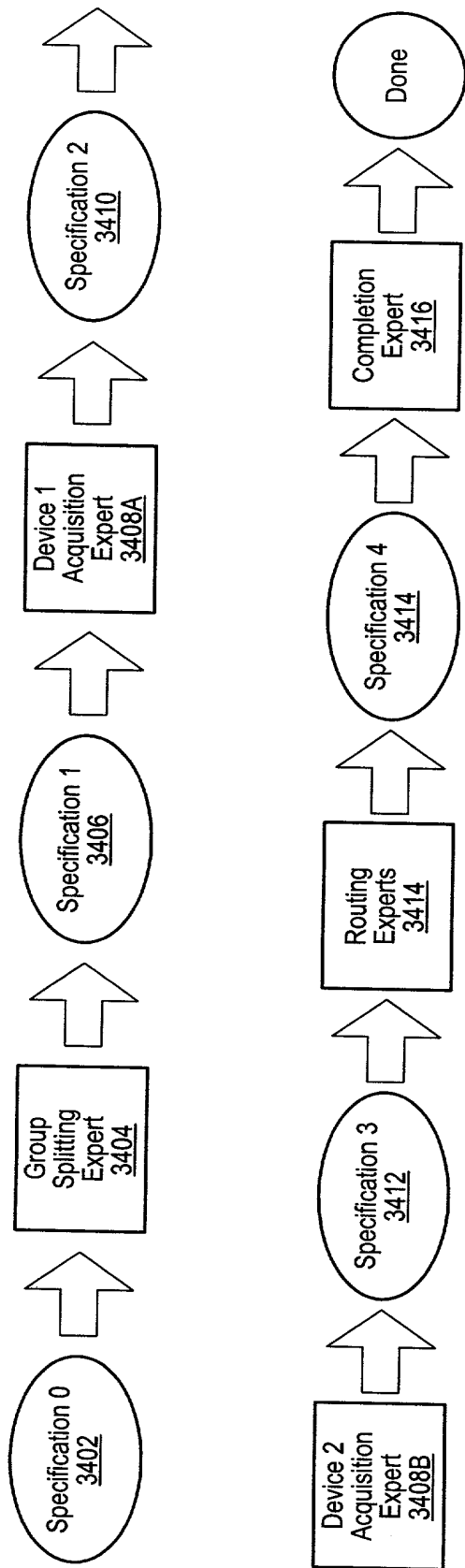


FIG. 34

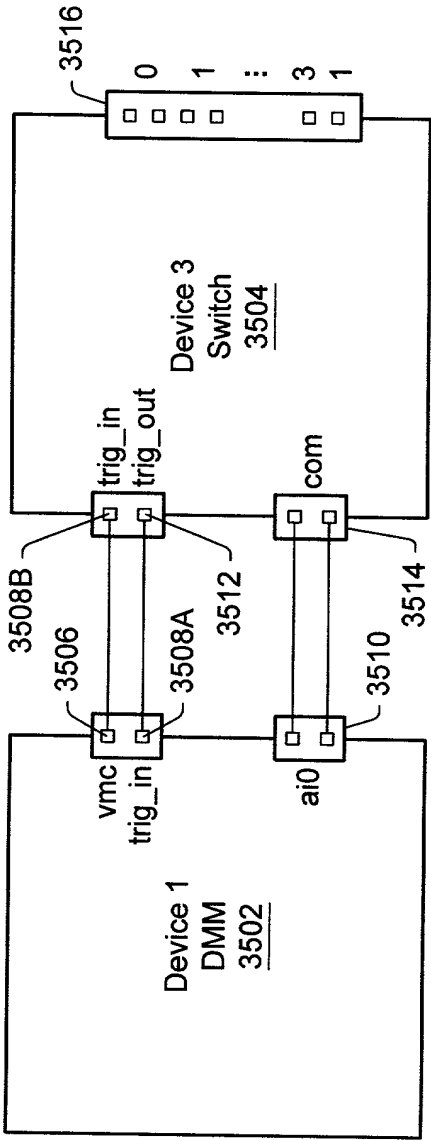


FIG. 35

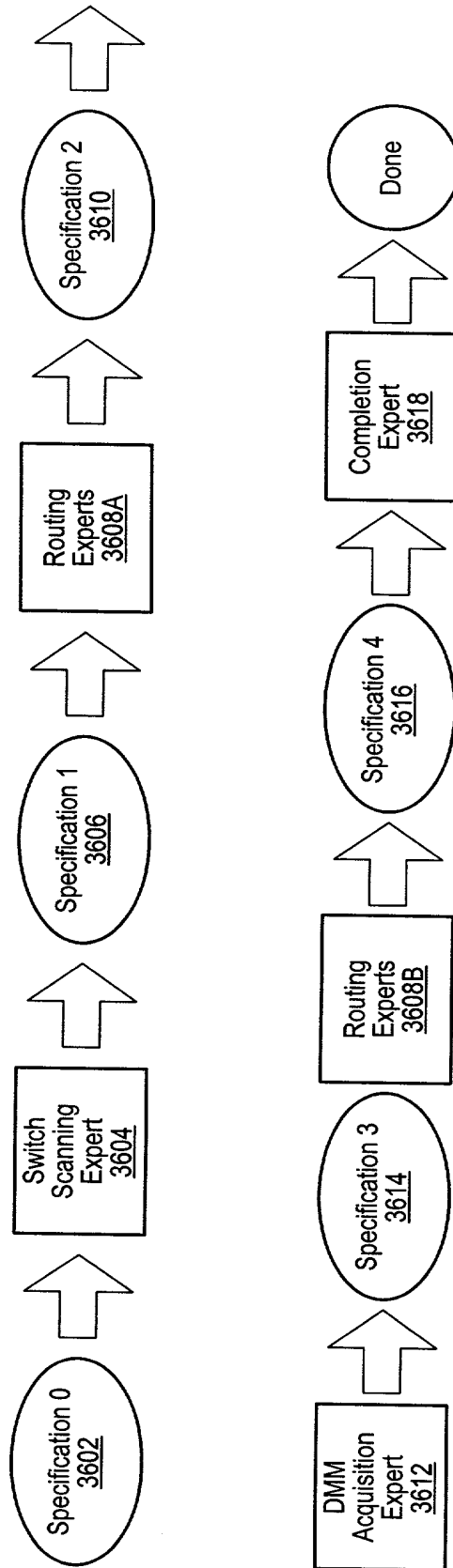


FIG. 36

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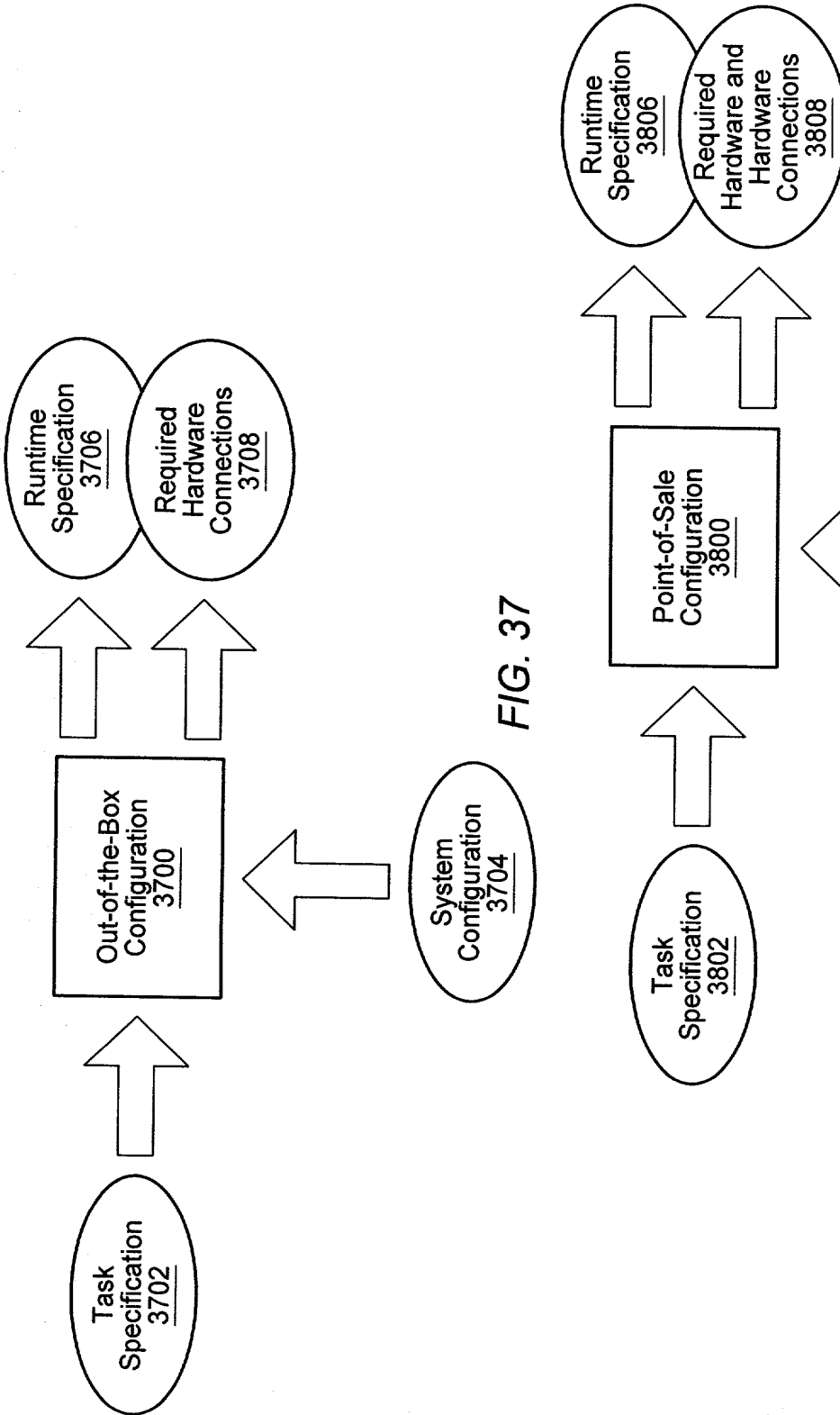


FIG. 37

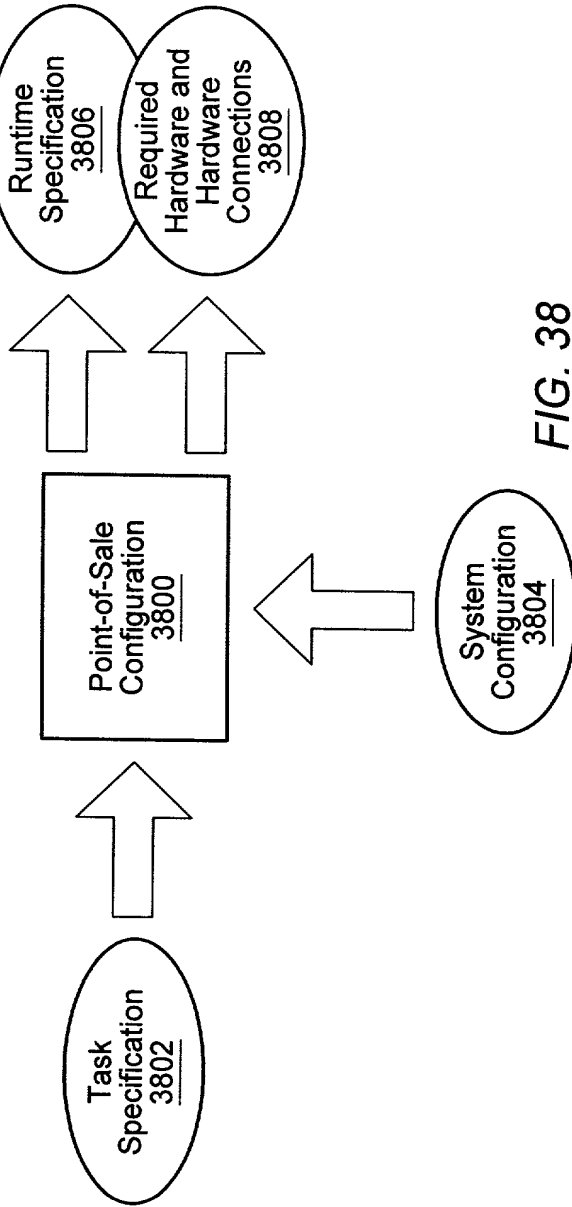


FIG. 38

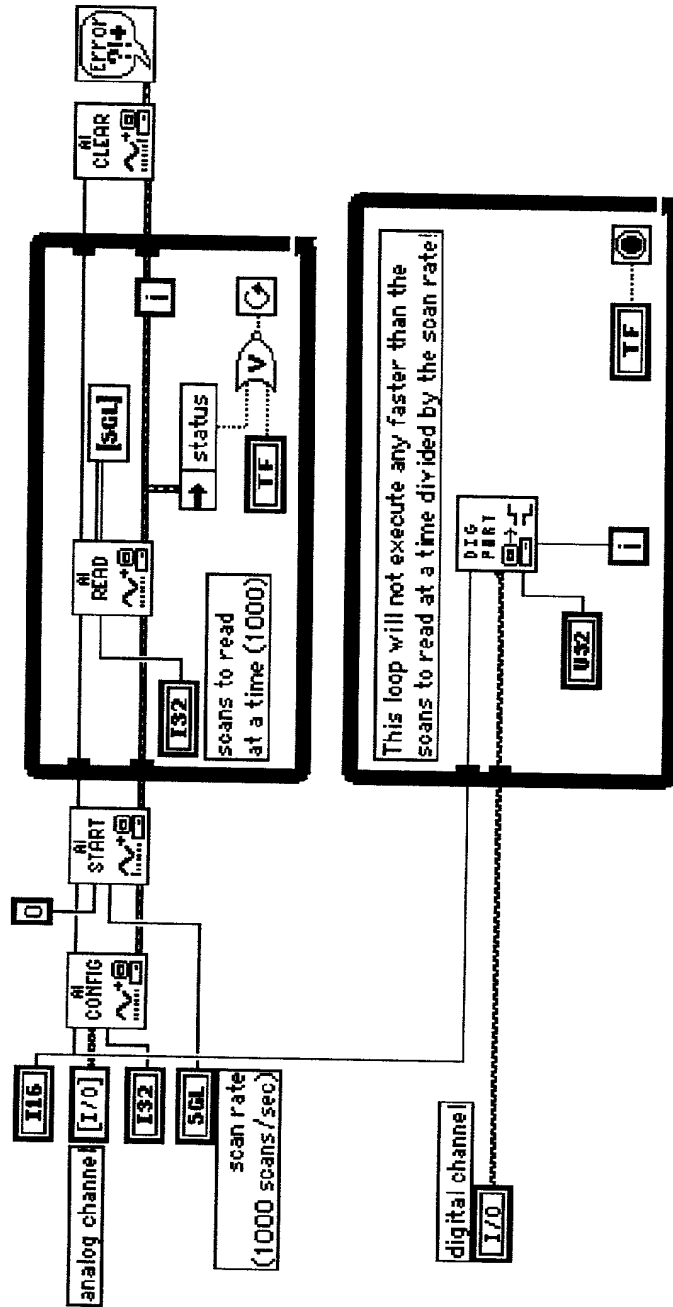
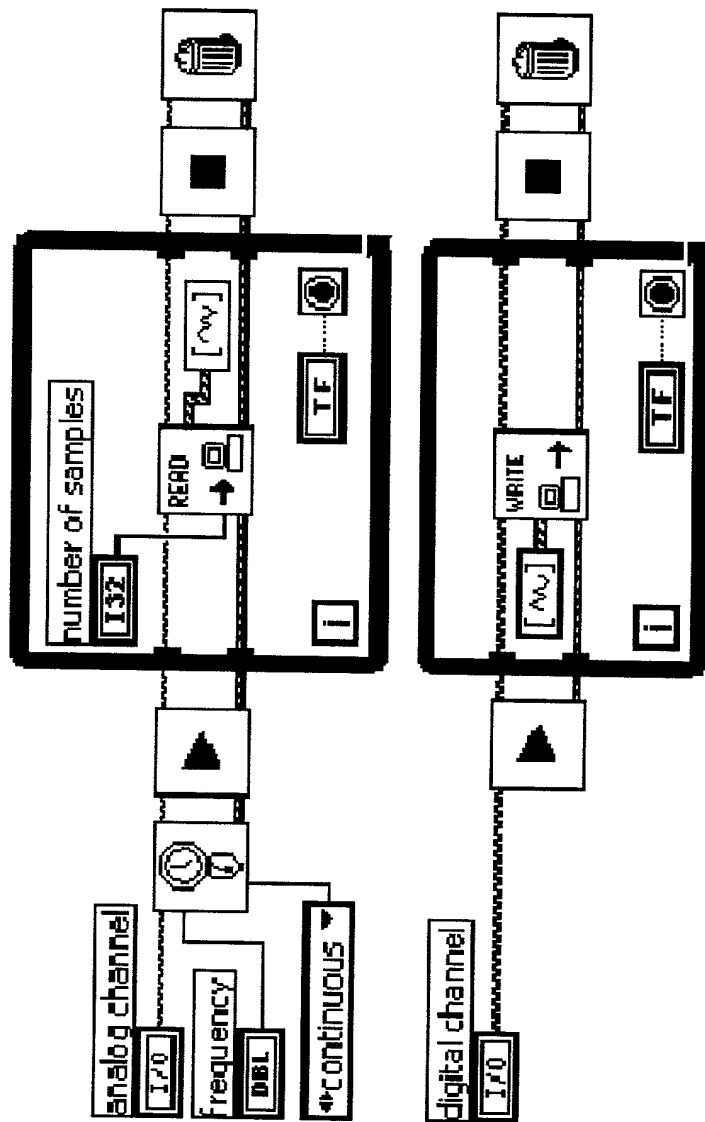


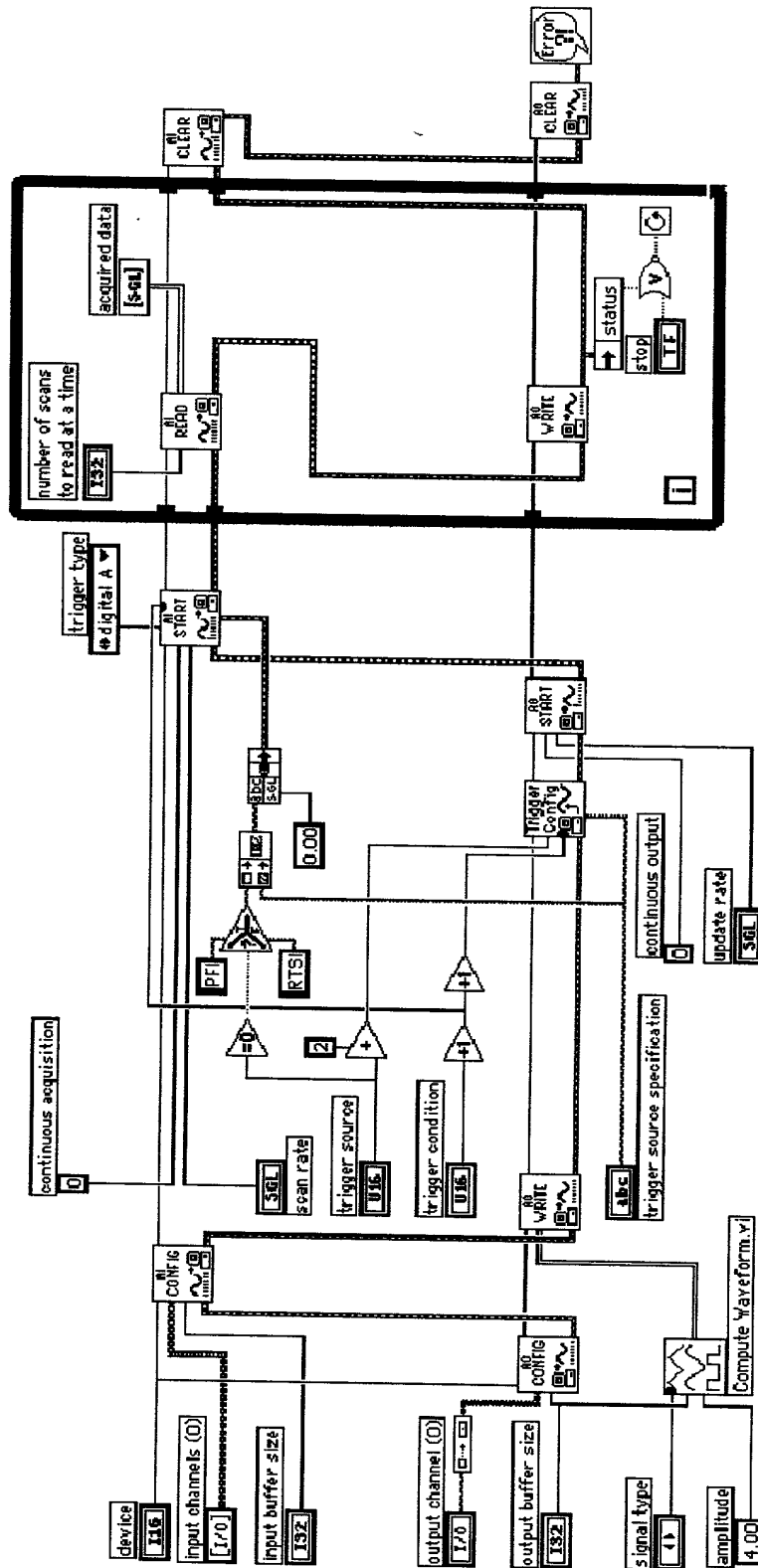
FIG. 39A
(Prior Art)

Simultaneous Buffered Analog Input And Single Point Digital Output With Single-Threaded Driver (Prior Art)



Simultaneous Buffered Analog Input And Single Point
Digital Output With Multi-Threaded Driver

FIG. 39B



Simultaneous Triggered Buffered A/AO (Prior Art)

FIG. 40A

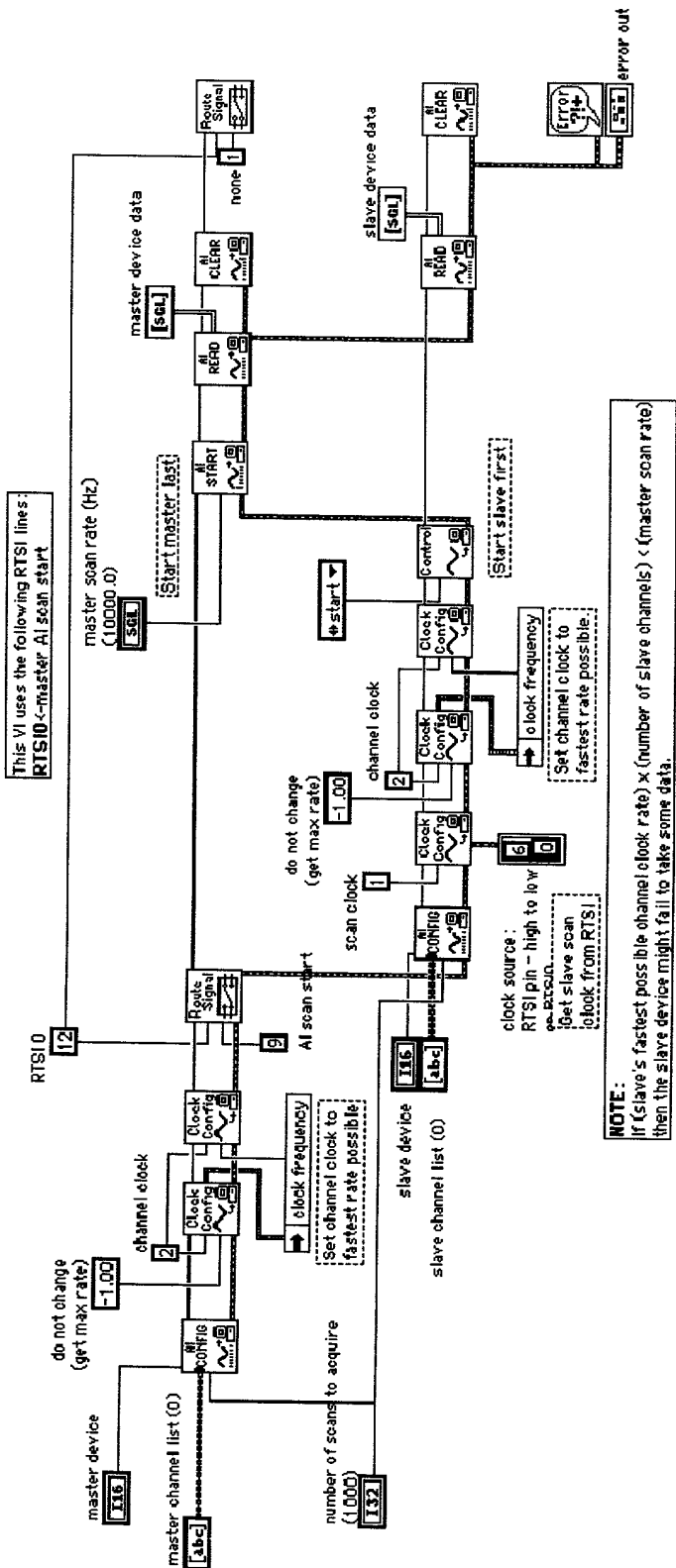
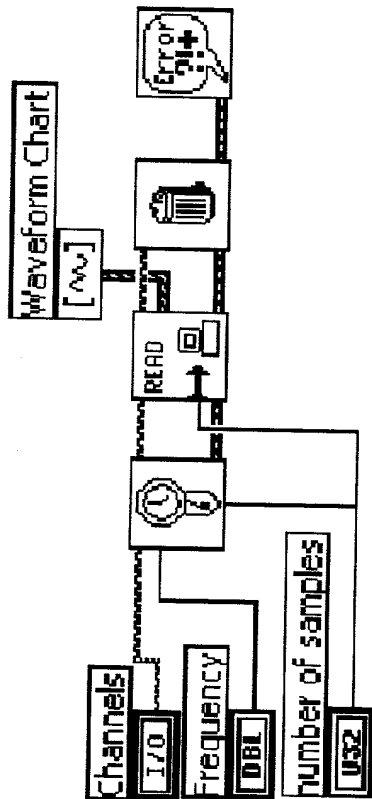


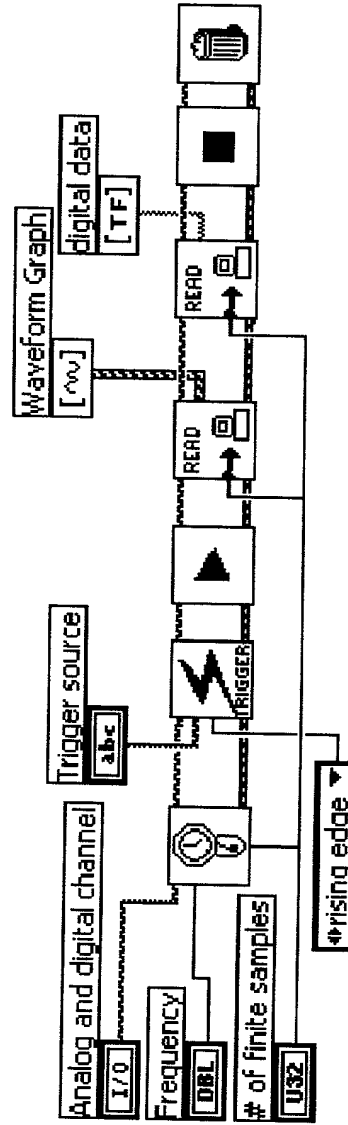
FIG. 41A

Sharing Scan Clock Across Two E-Series Devices (Prior Art)



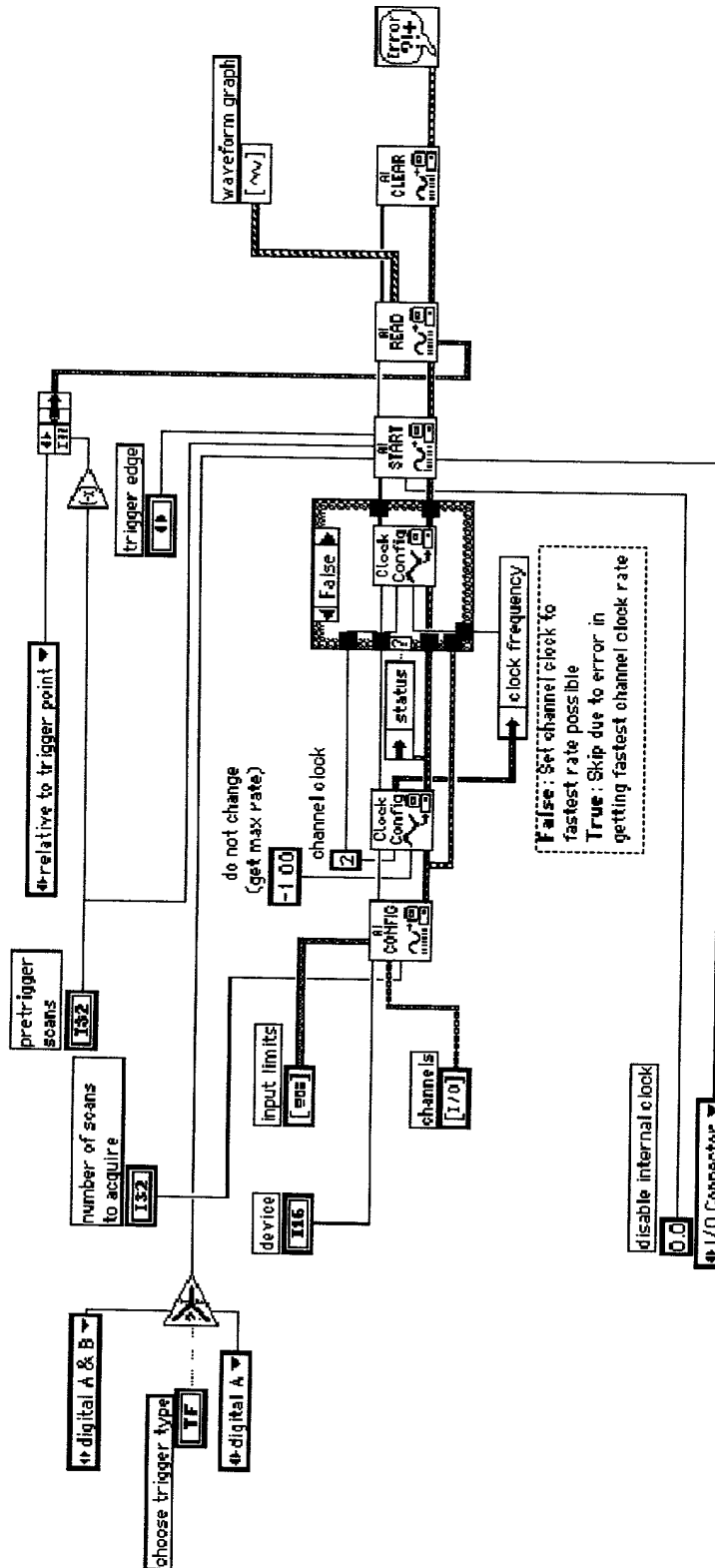
Sharing Scan Clock Across Two E-Series Devices

FIG. 41B



Sharing Clock And Trigger, Buffered AI & DI

FIG. 42



Acquire N Scans External Scan Clock Digital Trigger (Prior Art)

FIG. 43A
(Prior Art)

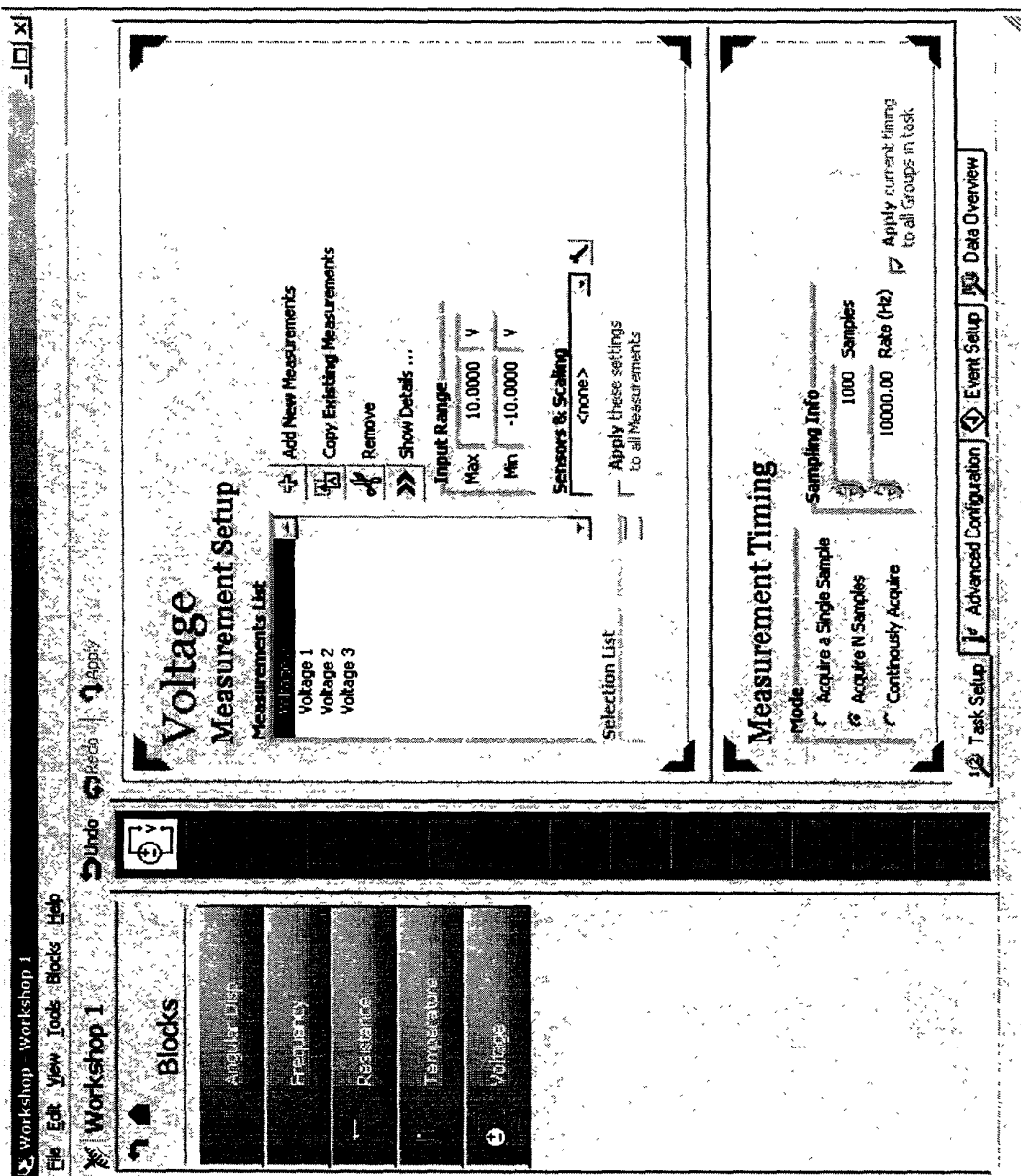
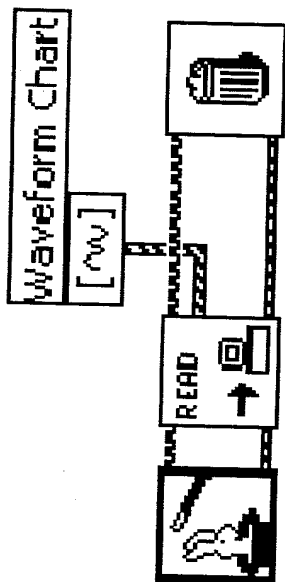
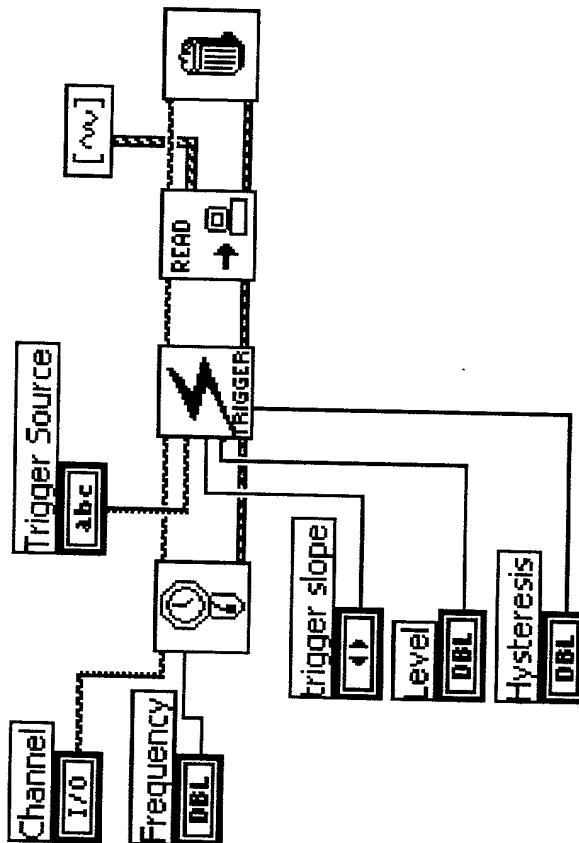


FIG. 43B



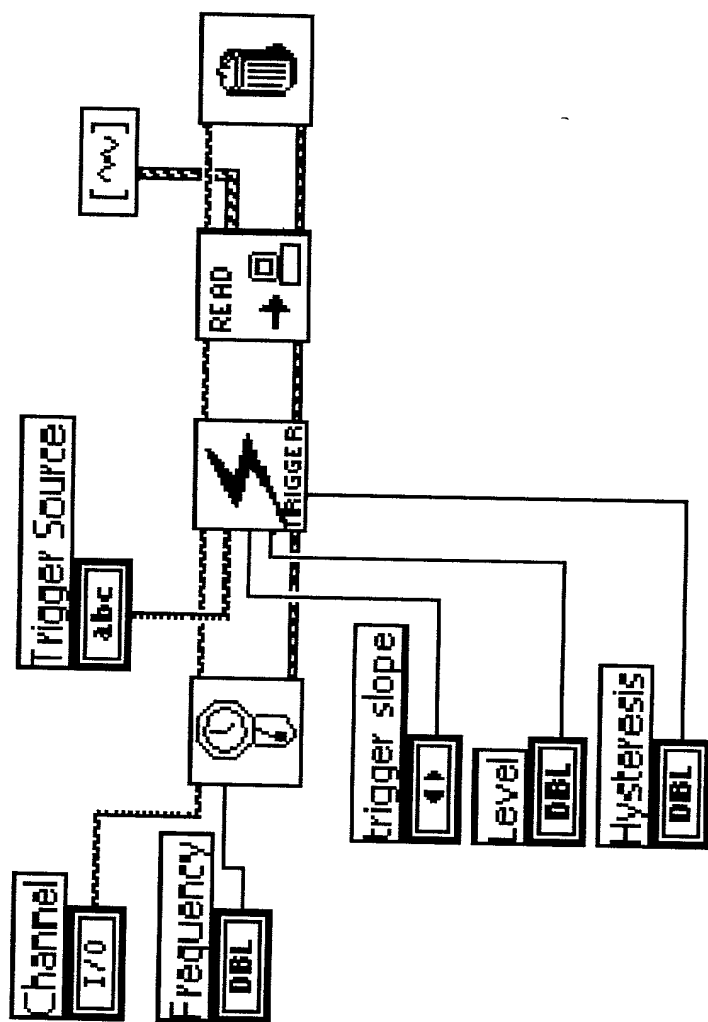
Acquire N Scans External Scan Clock Digital Trigger

FIG. 43D



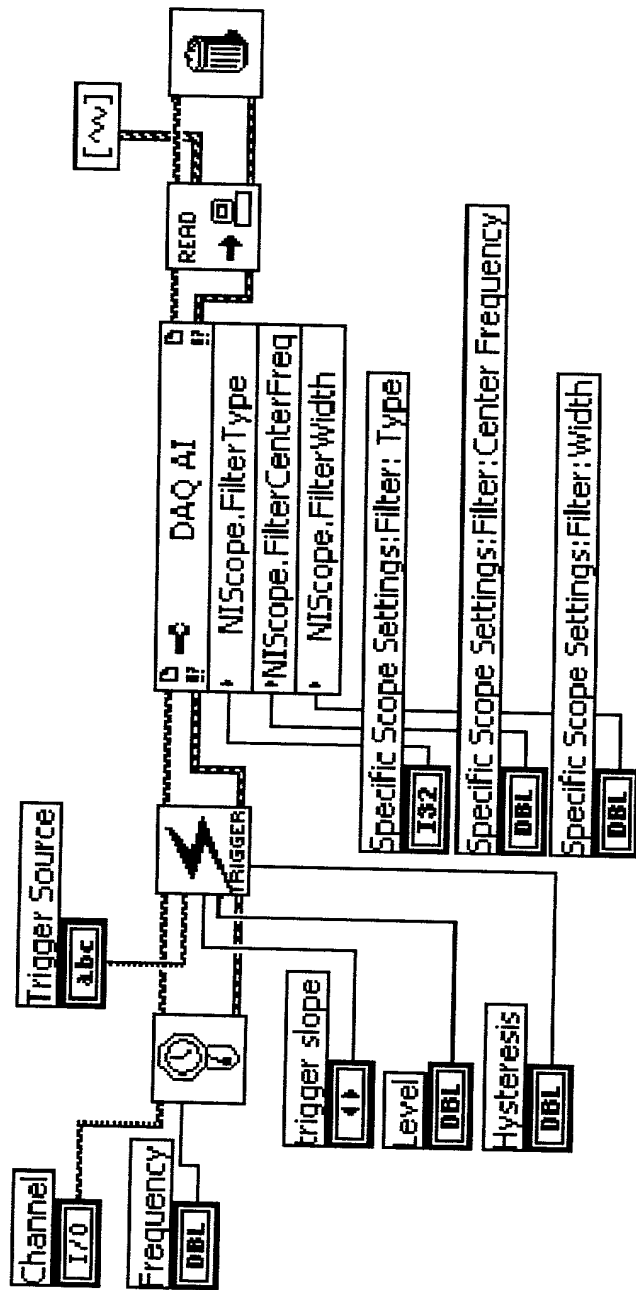
Triggered Acquisition With E-Series Device

FIG. 44A



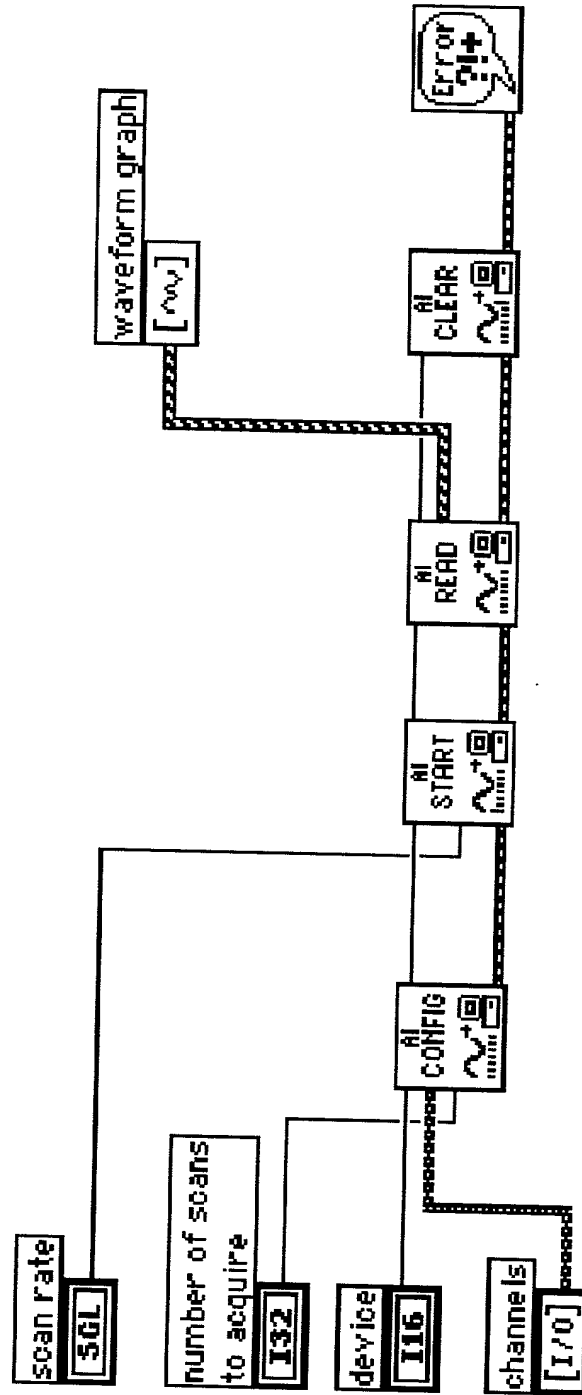
Triggered Acquisition With High Speed Digitizer

FIG. 44B



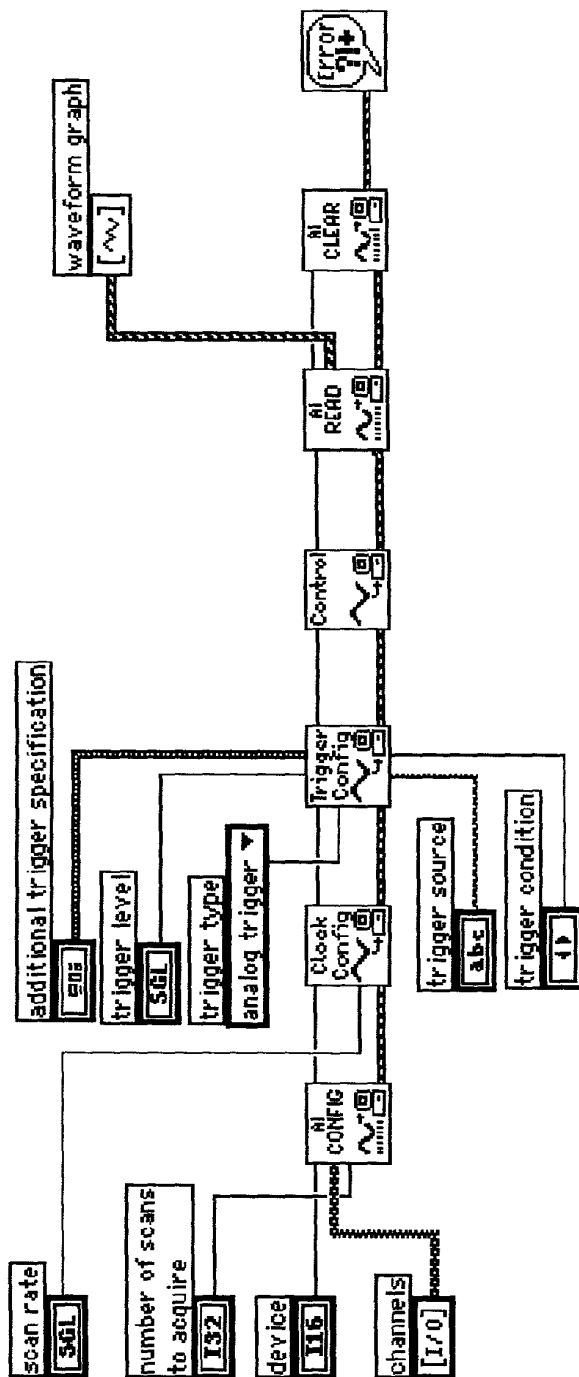
Triggered Acquisition With High Speed Digitizer With Filtering

FIG. 44C



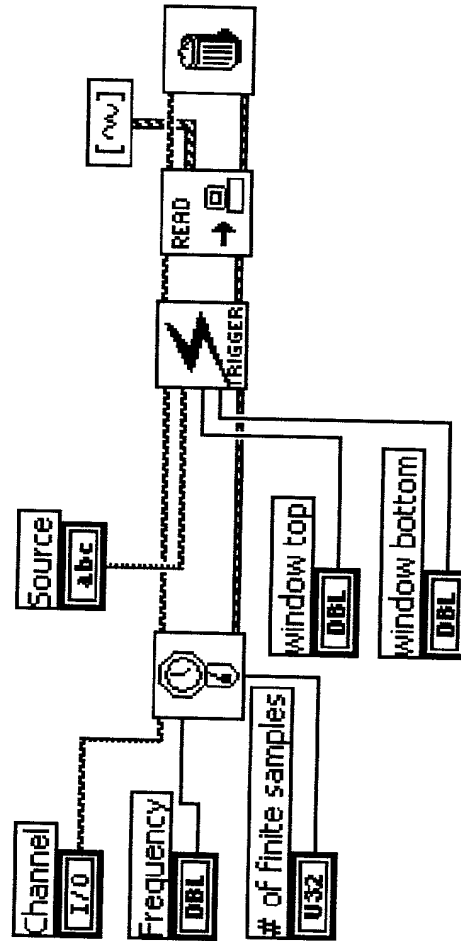
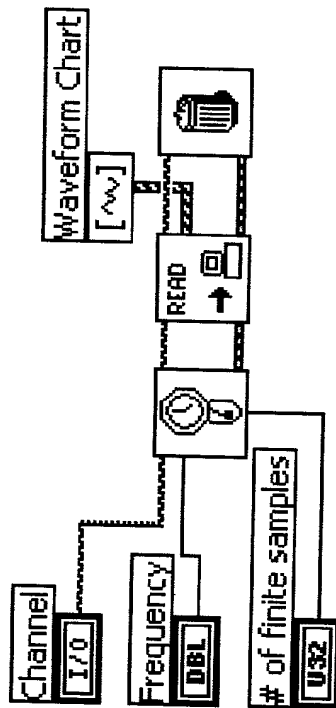
Intermediate Layer (Prior Art)

FIG. 45A



Changes For Analog Window Triggering (Prior Art)

FIG. 45B



Analog Window Triggering

FIG. 45C